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S1D13521 Epson/E-Ink Broadsheet

Hardware Functional Specification

SEIKO EPSON CORPORATION

Rev. 0.05

NOTICE

Table Of Contents

Chapter 1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13521 EPD Controller. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Display Subsystem Designers and Software Developers.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development. The latest revision can be downloaded at www.erd.epson.com.

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1.2 Overview Description

EPSON's S1D13521 controller provides a high performance, low cost, solution for current and future E Ink EPDs (Electronic Paper Displays). The controller greatly reduces CPU overhead by providing many functions that were previously handled by the Host.

The S1D13521 allows regional display updates which contribute to very responsive screen changes. The external memory interface is designed with support for 16/32-bit SDRAM bus widths. Additionally, the S1D13521 integrates support for current and future power management chips. All this is achieved with a lower parts cost than previous EPD controllers making the S1D13521 a prefect choice for new designs or design upgrades.

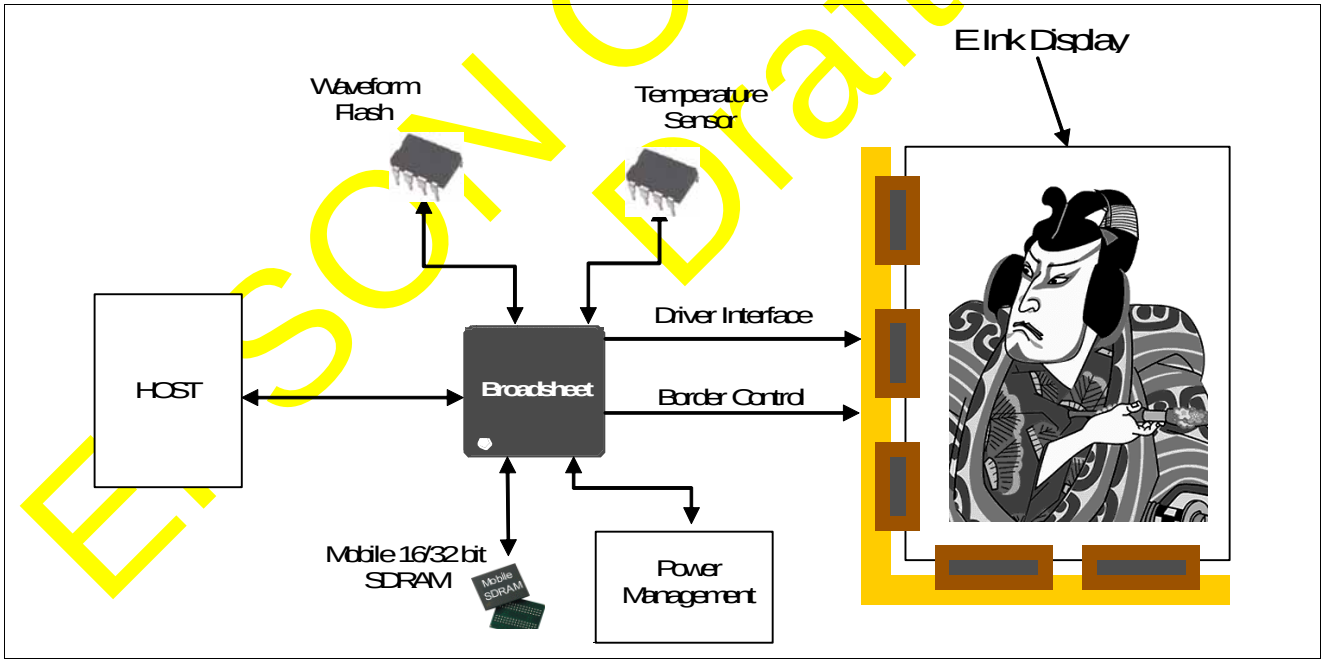


Figure 1-1: S1D13521 Overview

Chapter 2 Features

2.1 Direct Source and Gate Driver for Electrophoretic Display

- Supports up to 4096x4096 resolution
- 2 bpp, 3 bpp, 4 bpp, and 5 bpp grayscale
- Source Driver interfaces to the Micronix MX860 IC and compatible devices
  - Programmable up to 1024 pixels per IC
- Gate Driver interfaces to the Sharp LH1692 and compatible devices

2.2 16-Bit Host Interface

- Indirect 16-bit Host Bus Interface
- Registers can be accessed using Command Mode
- User programmed commands can be used to execute a pre-programmed series of commands

2.3 External Memory SDRAM Interface

- 16/32-bit SDRAM Interface
- Programmable Column Addressing Width
- Maximum operating frequency: 133MHz

2.4 Power Management IC

- Supports 3-wire Dialog DA8590 Active Matrix Power Management IC and compatible devices

2.5 Image Buffer Flexibility

- Host Writes can be rotated counter-clockwise by 90°, 180°, or 270°
- Host Write data input can use packed mode for high-speed transfers
- New image data can be loaded to the image buffer while display updates are in progress

2.6 I2C Thermal Sensor Temperature Reading

- Supports I2C sequence for temperature reading
- Supports National LM75 Digital Temperature Sensor and compatible devices

2.7 Serial Flash Memory Waveform Read

- Serial Flash Memory for Waveform Reads
- High Speed SPI Mode
- Waveform format: E Ink's waveform version 1 and version 2 (voltage controlled waveform)

2.8 Clock Source

- Internal Programmable PLL
- Single MHz clock input: CLKI
- Two terminal Crystal interface: OSCI/OSCO

2.9 Miscellaneous

- Sleep and Standby Power Save Modes
- General Purpose Input/Output pins are available (GPIO[1:0])
  - Interrupt pin associated with selectable GPIO inputs
- Package: PFBGA8UX 181-pin

Chapter 3 Block Diagram

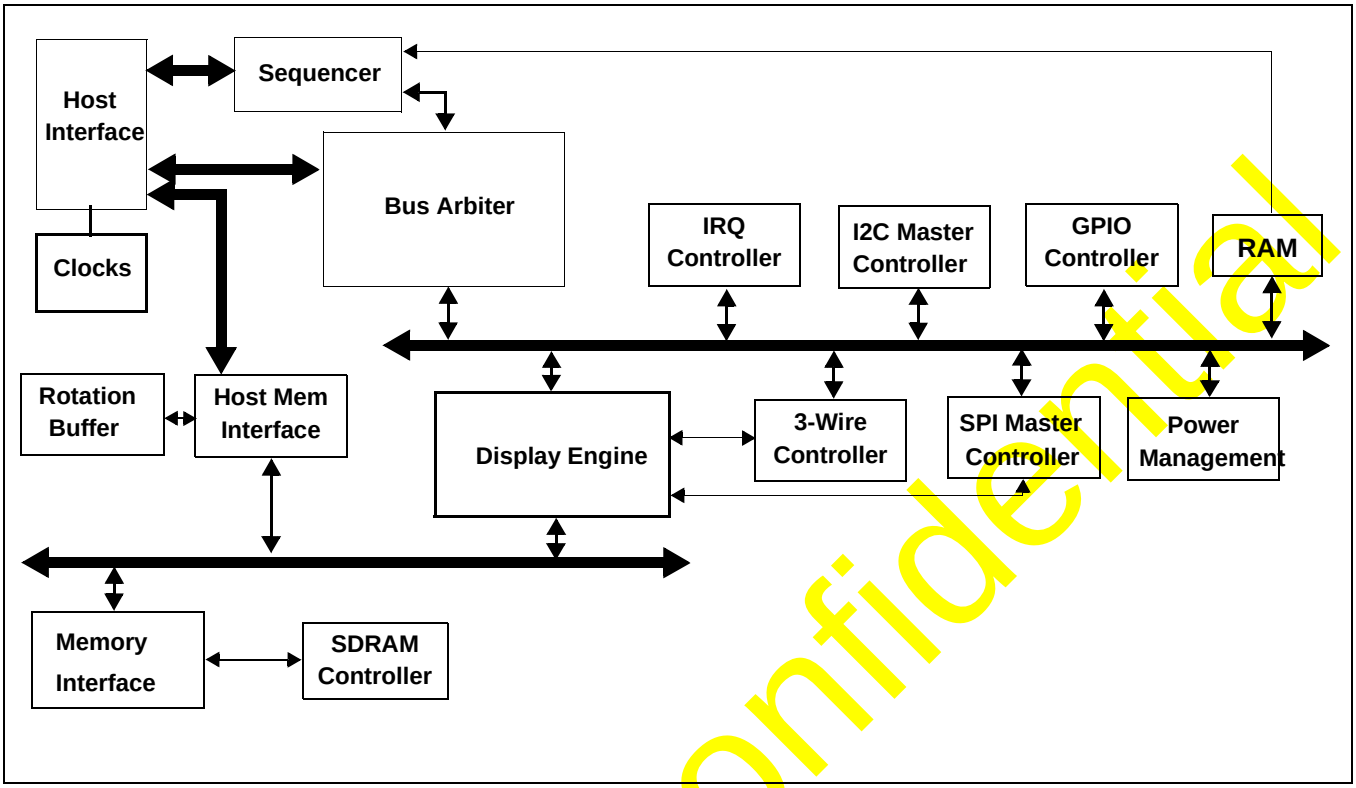


Figure 3-1: S1D13521 Block Diagram

3.1 Typical System Implementation

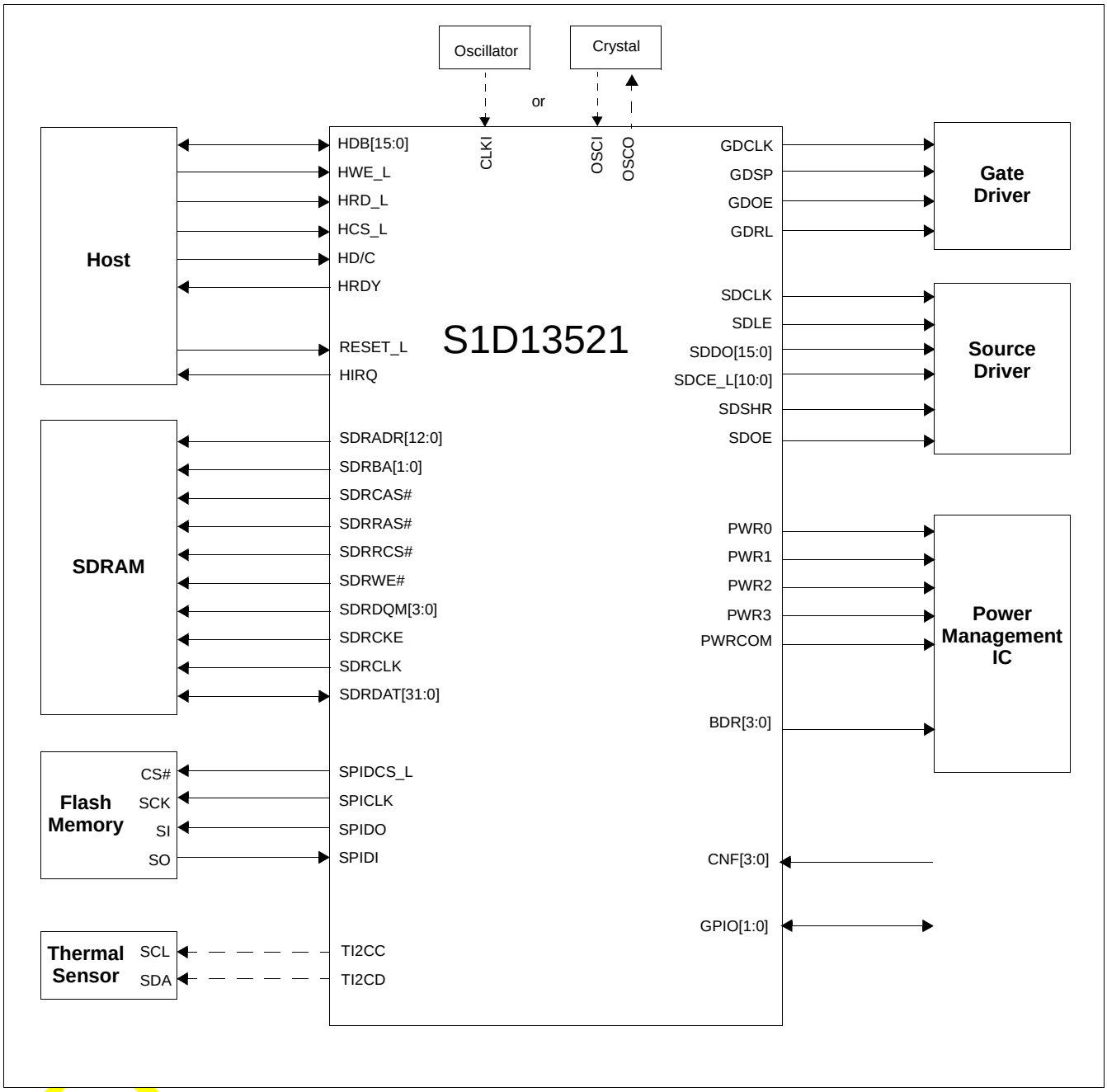


Figure 3-2: S1D13521 Typical System Implementation

Chapter 4 Pins

4.1 Pinout Diagram

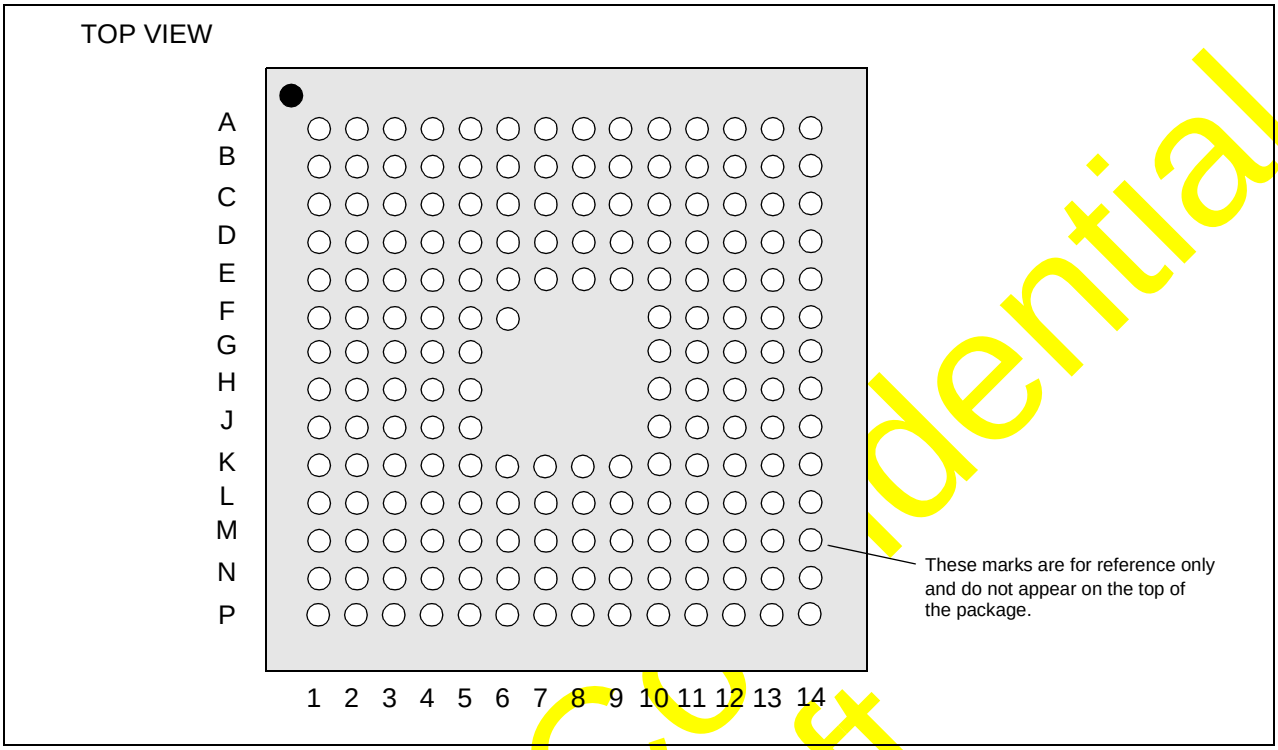
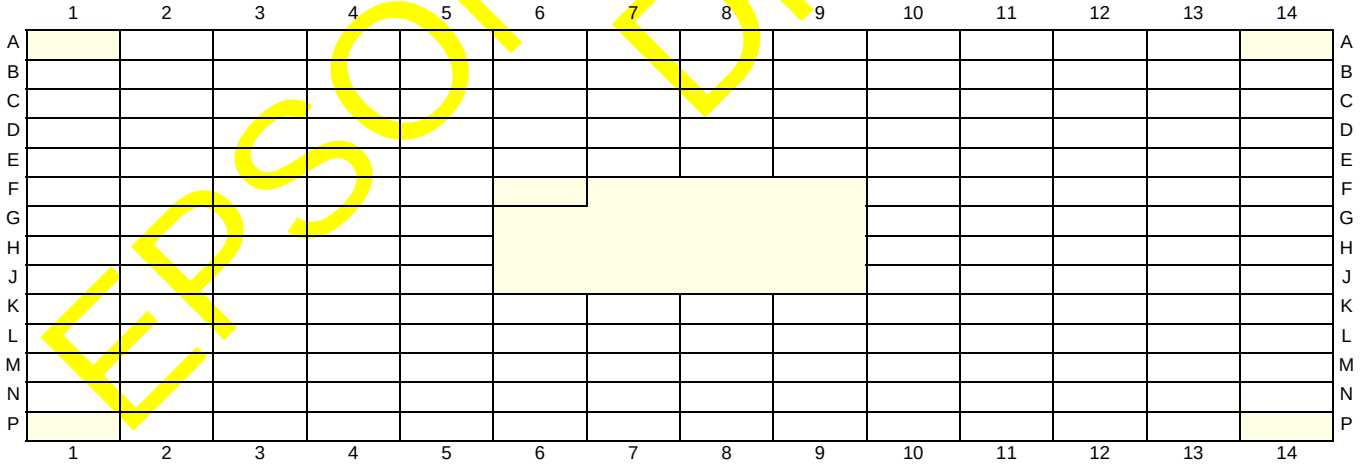


Figure 4-1: S1D13521 PFBGA8UX 181-pin Pin Mapping (Top View)

Table 4-1: S1D13521 PFBGA8UX 181-pin Pinout (Top View)



4.2 Pin Descriptions

Key:

Pin Types

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin

RESET# States

H	=	High level output
L	=	Low level output
Z	=	High Impedance (Hi-Z)
1	=	Pull-up resistor on input
0	=	Pull-down resistor on input
#	=	Active low level

Table 4-2: Cell Descriptions

Item	Description
IC	High voltage LVCMOS input buffer
ICS	High voltage LVCMOS Schmitt input buffer
ICD2	High voltage LVCMOS input buffer with pull-down (100kΩ@3.3V)
O	High voltage low noise output buffer (4mA@3.3V)
OH	High voltage high speed output buffer (4mA@3.3V)
BC	High voltage LVCMOS low noise bi-directional buffer (4mA@3.3V)
BCS	High voltage LVCMOS schmitt low noise bi-directional buffer (4mA@3.3V)
BCD2	High voltage LVCMOS low noise bi-directional buffer (4mA@3.3V) with pull-down (100kΩ@3.3V)
BCH	High voltage LVCMOS high speed bi-directional buffer (4mA@3.3V)
ILTR	Low voltage transparent input buffer
OLTR	Low voltage transparent output buffer

4.2.1 Shared Host Interface

Table 4-3: Shared Host Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
RESET_L	I		ICS	HIOVDD	—	This active low input sets all internal registers to their default states and forces all signals to their inactive states. When unused, this pin should be connected to HIOVDD. For RESET_L timing details, see Section 6.3, “RESET_L Timing” on page 31.
HIRQ	O		O	HIOVDD	L	This output pin is the Host IRQ.

4.2.2 Host Interface

Table 4-4: Host Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
HDB[15:0]	IO		BC	HIOVDD	Z	These pins are the shared command/parameter lines 15-0.
HWE_L	I		ICS	HIOVDD	—	This input pin is the Write Enable signal.
HRD_L	I		ICS	HIOVDD	—	This input pin is the Read Enable signal.
HCS_L	I		IC	HIOVDD	—	This input pin is the Chip Select signal.
HD/C	I		IC	HIOVDD	—	This input pin selects between Command (Low) and Parameter (High).
HRDY	IO		BC	HIOVDD	H	This active high pin is the Host interface Ready (or WAIT) signal.

4.2.3 SDRAM Interface

Table 4-5: SDRAM Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
SDRADR[12:0]	O		OH	SDRIOVDD	L	These output pins are the SDRAM Address pins.
SDRBA[1:0]	O		OH	SDRIOVDD	L	These output pins are the SDRAM Bank Address pins.
SDRCAS#	O		OH	SDRIOVDD	H	This output pin is the SDRAM CAS# pin.
SDRRAS#	O		OH	SDRIOVDD	H	This output pin is the SDRAM RAS# pin.
SDRRCS#	O		OH	SDRIOVDD	L	This output pin is the SDRAM CS# pin.
SDRWE#	O		OH	SDRIOVDD	H	This output pin is the SDRAM WE# pin.
SDRDQM[3:0]	O		OH	SDRIOVDD	H	These output pins are the SDRAM DQM pins.
SDRCKE	O		OH	SDRIOVDD	H	This output pin is the SDRAM CKE pin.
SDRCLK	O		OH	SDRIOVDD	H	This output pin is the SDRAM CLK pin.
SDRDAT[31:0]	IO		BCH	SDRIOVDD	L	These input/output pins are the SDRAM DATA pins.

4.2.4 SPI Master Interface for Serial Flash

Table 4-6: SPI Master Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
SPIDCS_L	O		O	PPIOVDD	H	This output pin is the Slave Chip Select for the SPI interface.
SPICLK	O		O	PPIOVDD	L	This output pin is the Slave Clock for the SPI interface.
SPIDO	O		O	PPIOVDD	L	This pin is the data output for the SPI interface.
SPIDI	I		IC	PPIOVDD	—	This pin is the data input for the SPI interface.

4.2.5 I2C Master Interface for Thermal Sensor

Table 4-7: I2C Master Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
TI2CC	IO		BCS	PPIOVDD	Z	This input/output pin is the I2C Master Serial Clock. If this pin is not used, it must be connected to PPIOVDD.
TI2CD	IO		BCS	PPIOVDD	Z	This input/output pin is the I2C Master Data. If this pin is not used, it must be connected to PPIOVDD.

4.2.6 Gate Driver Interface

Table 4-8: Gate Driver Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
GDCLK	O		O	PIOVDD	L	This output pin is the clock for the Gate Driver.
GDSP	O		O	PIOVDD	H	This output pin is the Gate Driver Start Pulse.
GDOE	O		O	PIOVDD	L	This output pin is the output enable for the Gate Driver.
GDRL	O		O	PIOVDD	L	This output pin is the Gate Driver Right or Left.

4.2.7 Source Driver Interface

Table 4-9: Source Driver Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
SDCLK	O		O	PIOVDD	L	This output pin is the clock for the Source Driver.
SDLE	O		O	PIOVDD	L	This output pin is the latch enable for the Source Driver.
SDDO[15:0]	O		O	PIOVDD	L	These are the data output pins for the Source Driver.
SDCE_L[10:9]	O		O	PIOVDD	H	These output pins are the Source Driver Chip Enables 10-9.
SDCE_L[8:0]	O		O	PIOVDD	H	These output pins are the Source Driver Chip Enables 8-0. For details on the configurability of these pins, refer to Section 10.3.15, “Display Engine: Driver Configurations” on page 123 (see REG[030Ch]) and Section 6.5.2, “Interpreted Source Driver Timings” on page 36.
SDSHR	O		O	PIOVDD	L	This output pin is the Source Driver Shift Right Enable.
SDOE	O		O	PIOVDD	L	This output pin is the output enable for the Source Driver.

4.2.8 Power Switches Control Interface

The power control interface signals have dual function pins.
1. Power sequence output (default power-on function)
2. 3-wire Dialog DA8590 Active Matrix Power Management IC and compatible devices

Table 4-10: Power Switches Control Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
PWR0/ DAPWRALL	IO		BC	PWIOVDD	L	These input/output pins have multiple functions. • Power Control Signal 0 (PWR0). For timing details, see Section 6.6.1, “Power Pin Transition Sequence for PWR[3:0]” on page 43. • 3-wire Power All Pin output (DAPWRALL)
PWR1/DACLK	IO		BC	PWIOVDD	L	These input/output pins have multiple functions. • Power Control Signal 1 (PWR1). For timing details, see Section 6.6.1, “Power Pin Transition Sequence for PWR[3:0]” on page 43. • 3-wire Serial Clock (DACLK)
PWR2/DADIO	IO		BC	PWIOVDD	L	These input/output pins have multiple functions. • Power Control Signal 2 (PWR2). For timing details, see Section 6.6.1, “Power Pin Transition Sequence for PWR[3:0]” on page 43. • 3-wire data tri-state input/output (DADIO)
PWR3/ DACEB	IO		BC	PWIOVDD	L	These input/output pins have multiple functions. • Power Control Signal 3 (PWR3). For timing details, see Section 6.6.1, “Power Pin Transition Sequence for PWR[3:0]” on page 43. • 3-wire active low enable (DACEB)
PWRCOM	O		O	PWIOVDD	L	Display Common Power Signals. For timing details, see Section 6.6.2, “Power Pin Transition Sequence for PWRCOM” on page 44.

4.2.9 Display Border Power Interface

Table 4-11: Display Border Power Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
BDR[3:0]	O		O	PWIOVDD	L	These output pins are the Display Border Power Signals.

4.2.10 Miscellaneous

Table 4-12: Miscellaneous Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
CLKI	I		ICS	HIOVDD	—	This pin is the clock input. For details on the clock structure, see Section Chapter 7, “Clocks” on page 45.
OSCI	I		ILTR	OSCVDD	—	This pin is the input for the 2-terminal crystal interface. When the internal oscillator is not used, this pin must be connected to OSCVDD. For details on the clock structure, see Section Chapter 7, “Clocks” on page 45.
OSCO	O		OLTR	OSCVDD	H	This pin is the output for the 2-terminal crystal interface. When the internal oscillator is not used, this pin must be left unconnected. For details on the clock structure, see Section Chapter 7, “Clocks” on page 45.
CNF[3:0]	I		IC	HIOVDD	—	These input pins are used for configuring the S1D13521 and must be connected to either HIOVDD or VSS. The states of these pins are latched at RESET_L. For a summary of configuration options, see Section 4.3, “Configuration Pins” on page 22.
GPIO[1:0]	IO		BCD2	HIOVDD	Z	These are the General Purpose Input/Output pins.
TESTEN	I		ICD2	HIOVDD	—	This input pin is the Test Enable pin and is used for production test only. This pin should be left unconnected for normal operation.
SCANEN	I		ICD2	HIOVDD	—	This input pin is the Scan Enable pin and is used for production test only. This pin should be left unconnected for normal operation.
VCP	O		OLTR	PLLVDD	—	This output pin is for production test only and must be left unconnected for normal operation.

4.2.11 Power and Ground

Table 4-13: Power And Ground Pin Descriptions

Pin Name	Type	PFBGA Pin#	Cell	Power	RESET_L State	Description
HIOVDD	P	2 balls	P	1.65-3.6V	—	IO power supply for the Host interface
SDRIOVDD	P	4 balls	P	1.8/3.3V	—	IO power supply for the SDRAM interface
PPIOVDD	P	1 ball	P	1.65-3.6V	—	IO power supply for the SPI and I2C interface
PWIOVDD	P	1 ball	P	1.65-3.6V	—	IO power supply for power switch & Display border control
PIOVDD	P	2 balls	P	1.65-3.6V	—	IO power supply for Source and Gate Driver
COREVDD	P	6 balls	P	1.8V	—	Core power supply
VSS	P	15 balls	P	0	—	GND for HIOVDD, SDRIOVDD, SPIOVDD, PIOVDD, TSIOVDD, PWIOVDD, DBIOVDD, PIOVDD, and COREVDD
PLLVDD	P	1 ball	P	1.8V	—	PLL power supply
PLLVSS	P	1 ball	P	0	—	GND for PLLVDD
OSCVDD	P	1 ball	P	1.8V	—	OSC power supply
OSCVSS	P	1 ball	P	0	—	GND for OSCVDD

4.3 Configuration Pins

The S1D13521 has four configuration pins, CNF[3:0], which should be pulled high or low based on the following table.

Table 4-14: Configuration Pin Summary

CNF[3:0]	1 (connected to HIOVDD)	0 (connected to VSS)
CNF3	HRDY only driven when HCS_L is asserted	HRDY is always driven
CNF2	OSCI/OSCO is the source for the Input Clock.	CLKI is the source for the Input Clock.
CNF1	Reserved. This pin must be connected to HIOVDD.	
CNF0	Reserved. This pin must be connected to VSS.	

4.4 Pin Mapping

4.4.1 Source Driver Interface

The Source Driver output width is dependent on the Pixel Output Count Select bit (see REG[030Ch] bit 11).

Table 4-15: Source Driver Interface Bitwidth Select

Pin Name	Pixel Output Count Select = 0 (4 pixels per SDCLK)		Pixel Output Count Select = 1 (8 pixels per SDCLK)	
	2-bit Voltage Level Control	4-bit Voltage Level Control	2-bit Voltage Level Control	4-bit Voltage Level Control
SDCLK	SDCLK	SDCLK	SDCLK	No Supported Mode
SDLE	SDLE	SDLE	SDLE	
SDDO[1:0]	Pixel 0[1:0]	Pixel 0[1:0]	Pixel 0[1:0]	
SDDO[3:2]	Pixel 1[1:0]	Pixel 0[2:3]	Pixel 1[1:0]	
SDDO[5:4]	Pixel 2[1:0]	Pixel 1[1:0]	Pixel 2[1:0]	
SDDO[7:6]	Pixel 3[1:0]	Pixel 1[2:3]	Pixel 3[1:0]	
SDDO[9:8]	driven 0	Pixel 2[1:0]	Pixel 4[1:0]	
SDDO[11:10]	driven 0	Pixel 2[2:3]	Pixel 5[1:0]	
SDDO[13:12]	driven 0	Pixel 3[1:0]	Pixel 6[1:0]	
SDDO[15:14]	driven 0	Pixel 3[2:3]	Pixel 7[1:0]	
SDCE_L[10:0]	SDCE_L[10:0]	SDCE_L[10:0]	SDCE_L[10:0]	
SDSHR	SDSHR	SDSHR	SDSHR	
SDOE	SDOE	SDOE	SDOE	

4.4.2 Border Pin Interface

Table 4-16: Border Pin Interface Bitwidth Select

Pin Name	2-bit Voltage Level Control	4-bit Voltage Level Control
BDR[1:0]	Border Value[1:0]	Border Value[1:0]
BDR[3:2]	Driven 0	Border Value[2:3]

Chapter 5 D.C. Characteristics

5.1 Absolute Maximum Ratings

Table 5-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
Core V_{DD}	Core Supply Voltage	V_{SS} - 0.3 ~ 2.5	V
PLL V_{DD}	PLL Supply Voltage	V_{SS} - 0.3 ~ 2.5	V
OSC V_{DD}	OSC Supply Voltage	V_{SS} - 0.3 ~ 2.5	V
HIO V_{DD}	Host IO Supply Voltage	V_{SS} - 0.3 ~ 4.0	V
PIO V_{DD}	Gate/Source IO Supply Voltage	V_{SS} - 0.3 ~ 4.0	V
SDRIO V_{DD}	SDRAM IO Supply Voltage	V_{SS} - 0.3 ~ 4.0	V
PPIO V_{DD}	SPI and I2C IO Supply Voltage	V_{SS} - 0.3 ~ 4.0	V
PWIO V_{DD}	Power Switch Control IO Supply Voltage	V_{SS} - 0.3 ~ 4.0	V
V_{IN}	Input Signal Voltage	V_{SS} - 0.3 ~ *IO V_{DD} + 0.5	V
V_{OUT}	Output Signal Voltage	V_{SS} - 0.3 ~ *IO V_{DD} + 0.5	V
I_{OUT}	Output Signal Current	±10	mA
T_{STG}	Storage Temperature	-65 ~ 150	°C

Note
V_{SS} = 0 V
Core V_{DD}, PLL V_{DD}, OSC V_{DD} ≤ *IOV_{DD}

5.2 Recommended Operating Conditions

Table 5-2: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
Core V_{DD}	Core Supply Voltage	V_{SS} = 0 V	1.65	1.80	1.95	V
PLL V_{DD}	PLL Supply Voltage	V_{SS} = 0 V	1.65	1.80	1.95	V
OSC V_{DD}	OSC Supply Voltage	V_{SS} = 0 V	1.65	1.80	1.95	V
HIO V_{DD}	Host IO Supply Voltage	V_{SS} = 0 V	1.65	—	3.60	V
PIO V_{DD}	Gate/Source IO Supply Voltage	V_{SS} = 0 V	1.65	—	3.60	V
SDRIO V_{DD}	SDRAM IO Supply Voltage	V_{SS} = 0 V	1.65	1.80	1.95	V
		V_{SS} = 0 V	2.70	3.30	3.60	V
PPIO V_{DD}	SPI and I2C IO Supply Voltage	V_{SS} = 0 V	1.65	—	3.60	V
PWIO V_{DD}	Power Switch Control IO Supply Voltage	V_{SS} = 0 V	1.65	—	3.60	V
V_{IN}	Input Voltage	—	V_{SS}	—	*IO V_{DD}	V
T_{OPR}	Operating Temperature	—	-40	25	85	°C

5.3 Electrical Characteristics

Table 5-3: Electrical Characteristics for IO V_{DD} = 1.8V ± 0.15V

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions	—	TBD	—	µA
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Output Leakage Current	—	-5	—	5	µA
I_{OH}	High Level Output Current	IOV_{DD} = min V_{OH} = IO V_{DD} - 0.4 V	-2	—	—	mA
I_{OL}	Low Level Output Current	IOV_{DD} = min V_{OL} = 0.4 V	2	—	—	mA
V_{IH}	High Level Input Voltage	LVCMOS Level IO V_{DD} = max	1.27	—	IO V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage	LVCMOS Level IO V_{DD} = min	-0.3	—	0.57	V
V_{T+}	Positive Trigger Voltage	LVCMOS Schmitt	0.58	—	1.46	V
V_{T-}	Negative Trigger Voltage	LVCMOS Schmitt	0.42	—	1.26	V
V_H	Hysteresis Voltage	LVCMOS Schmitt	0.17	—	—	V
R_{PU}	Pull-Up Resistance	V_{IN} = 0 V	96	240	600	kΩ
R_{PD}	Pull-Down Resistance	V_{IN} = IO V_{DD}	96	240	600	kΩ
C_I	Input Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF
C_O	Output Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF
C_{IO}	Bi-Directional Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF

Table 5-4: Electrical Characteristics for IO V_{DD} = 2.5V ± 0.2V

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions	—	TBD	—	µA
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Output Leakage Current	—	-5	—	5	µA
I_{OH}	High Level Output Current	IOV_{DD} = min V_{OH} = IO V_{DD} - 0.4 V	-3	—	—	mA
I_{OL}	Low Level Output Current	IOV_{DD} = min V_{OL} = 0.4 V	3	—	—	mA
V_{IH}	High Level Input Voltage	LVCMOS Level IO V_{DD} = max	1.7	—	IO V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage	LVCMOS Level IO V_{DD} = min	-0.3	—	0.7	V
V_{T+}	Positive Trigger Voltage	LVCMOS Schmitt	0.92	—	1.89	V
V_{T-}	Negative Trigger Voltage	LVCMOS Schmitt	0.58	—	1.48	V
V_H	Hysteresis Voltage	LVCMOS Schmitt	0.23	—	—	V
R_{PU}	Pull-Up Resistance	V_{IN} = 0 V	70	140	350	kΩ
R_{PD}	Pull-Down Resistance	V_{IN} = IO V_{DD}	70	140	350	kΩ
C_I	Input Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF
C_O	Output Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF
C_{IO}	Bi-Directional Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF

Table 5-5: Electrical Characteristics for IO V_{DD} = 3.3V ± 0.3V

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions	—	TBD	—	µA
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Output Leakage Current	—	-5	—	5	µA
I_{OH}	High Level Output Current	IOV_{DD} = min V_{OH} = IO V_{DD} - 0.4 V	-4	—	—	mA
I_{OL}	Low Level Output Current	IOV_{DD} = min V_{OL} = 0.4 V	4	—	—	mA
V_{IH}	High Level Input Voltage	LVCMOS Level IO V_{DD} = max	2.2	—	IO V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage	LVCMOS Level IO V_{DD} = min	-0.3	—	0.8	V
V_{T+}	Positive Trigger Voltage	LVCMOS Schmitt	1.2	—	2.52	V
V_{T-}	Negative Trigger Voltage	LVCMOS Schmitt	0.75	—	1.98	V
V_H	Hysteresis Voltage	LVCMOS Schmitt	0.3	—	—	V
R_{PU}	Pull-Up Resistance	V_{IN} = 0 V	50	100	240	kΩ
R_{PD}	Pull-Down Resistance	V_{IN} = IO V_{DD}	50	100	240	kΩ
C_I	Input Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF
C_O	Output Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF
C_{IO}	Bi-Directional Pin Capacitance	f = 1MHz, IO V_{DD} = 0V	—	—	6	pF

Table 5-6: Electrical Characteristics for CORE V_{DD}

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions	—	TBD	—	µA
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Output Leakage Current	—	-5	—	5	µA

Table 5-7: Electrical Characteristics for PLL V_{DD}

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DDS}	Quiescent Current	Quiescent Conditions	—	TBD	—	µA
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Output Leakage Current	—	-5	—	5	µA

Chapter 6 A.C. Characteristics

Conditions:
TBD

6.1 Clock Timing

6.1.1 Input Clocks

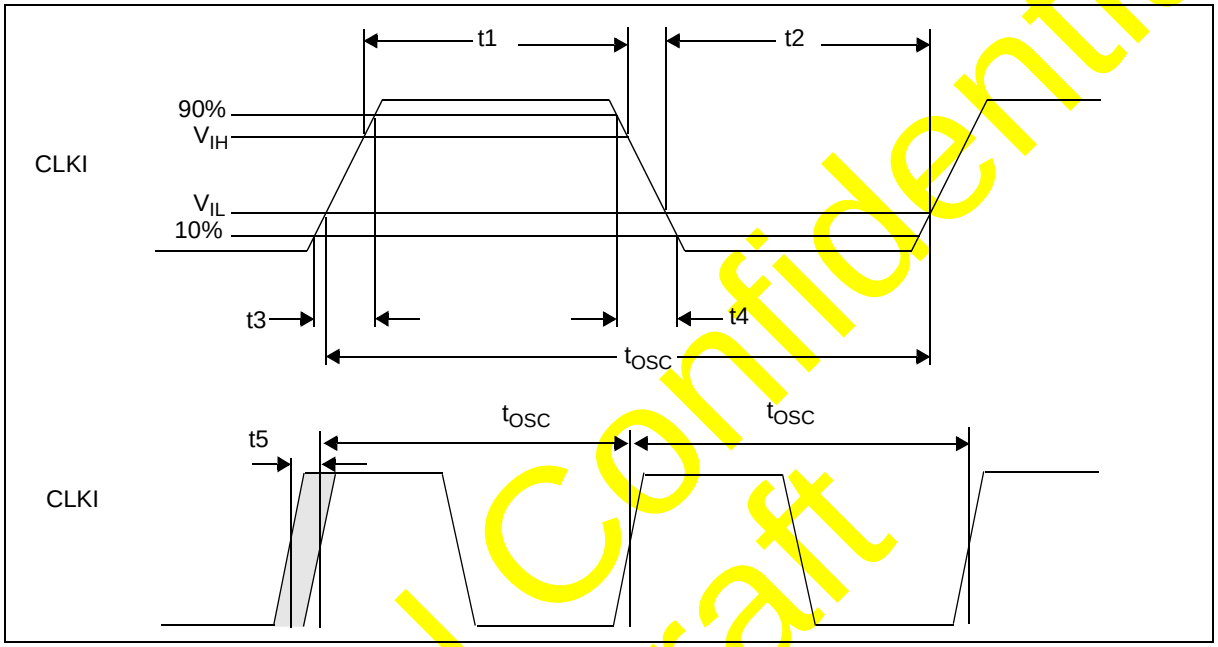


Figure 6-1 Clock Input Required (CLKI)

Table 6-1 Clock Input Requirements

Symbol	Parameter	Min	Typ	Max	Units
f_{OSC}	Input clock frequency of CLKI when PLL used for System Clock (see Note 6)	20	—	66.5	MHz
	Input clock frequency of CLKI when CLKI used for System Clock	0	—	TBD	MHz
	Input clock frequency of OSC when PLL used for System Clock (see Note 6)	24	—	27	MHz
t_{OSC}	Input clock period	—	$1/f_{OSC}$	—	µs
t1	Input clock pulse width high (see Note 5)	$0.4t_{OSC}$	—	$0.6t_{OSC}$	µs
t2	Input clock pulse width low (see Note 5)	$0.4t_{OSC}$	—	$0.6t_{OSC}$	µs
t3	Input clock rise time (10% - 90%)	—	—	500	ps
t4	Input clock fall time (90% - 10%)	—	—	500	ps
t5	Input clock period jitter (see notes 2 and 4)	-150		150	ps
t6 (see note 1)	Input clock cycle jitter (see notes 3 and 4)	-150		150	ps

1. t6 = 2 x t_{OSC}
2. The input clock period jitter is the displacement relative to the center period (reciprocal of the center frequency).
3. The input clock cycle jitter is the difference in period between adjacent cycles.
4. The jitter characteristics must satisfy both the t5 and t6 characteristics
5. Input Duty cycle is not critical and can be 40/60
6. To achieve the maximum possible PLL output frequency, the input source frequency must be evenly divisible into 133 MHz. For further details on programming the PLL, see Section 10.3.2, “Clock Configuration Registers” on page 83.

6.1.2 PLL Clock

The PLL circuit is an analog circuit and is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible. The jitter of the input clock waveform should be as small as possible.

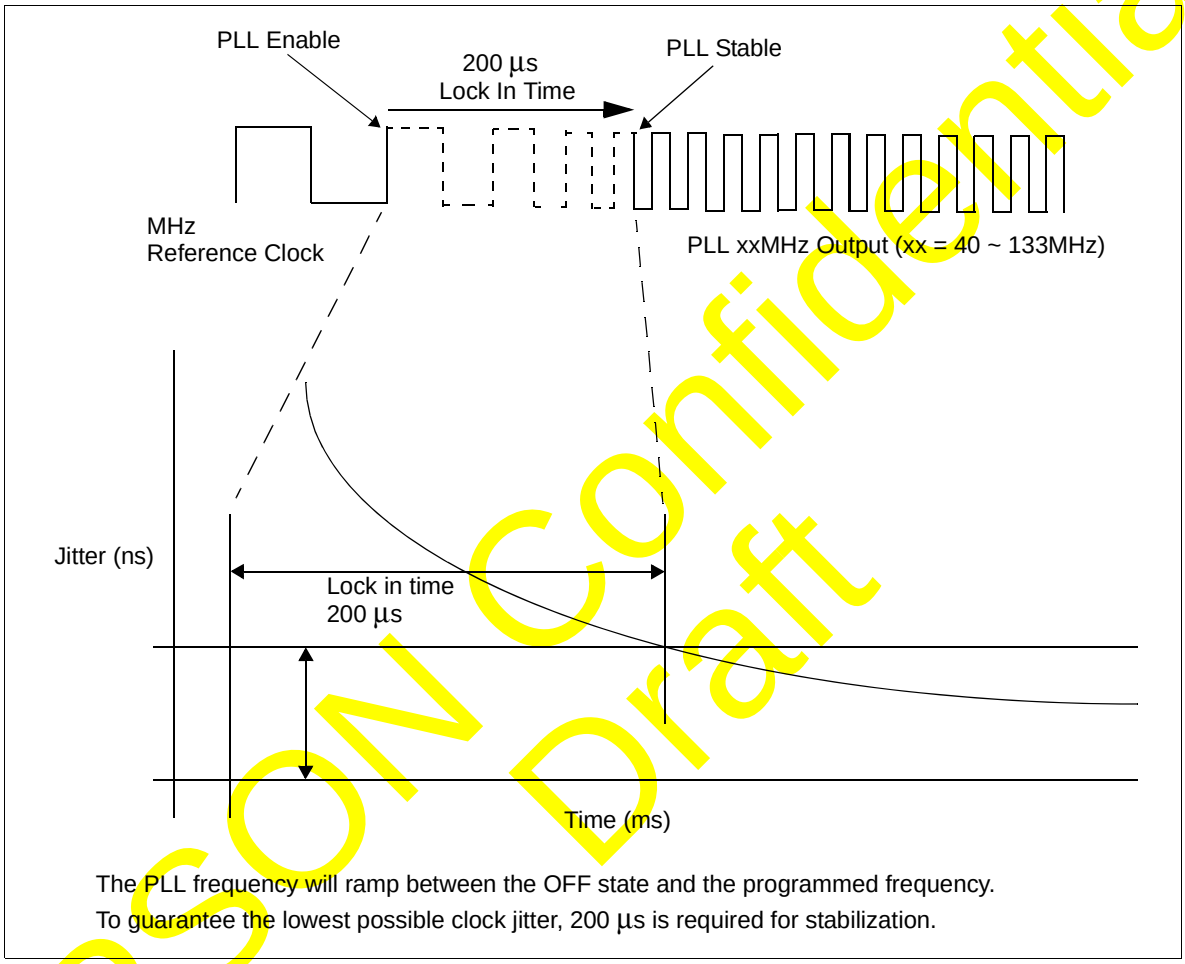


Figure 6-2: PLL Start-Up Time

Table 6-2: PLL Clock Requirements

Symbol	Parameter	Min	Max	Units
f_{PLL}	PLL output clock frequency	40	133	MHz
t_{PStal}	PLL output stable time	—	200	µs

6.2 Power Supply Sequence

6.2.1 Power-On Sequence

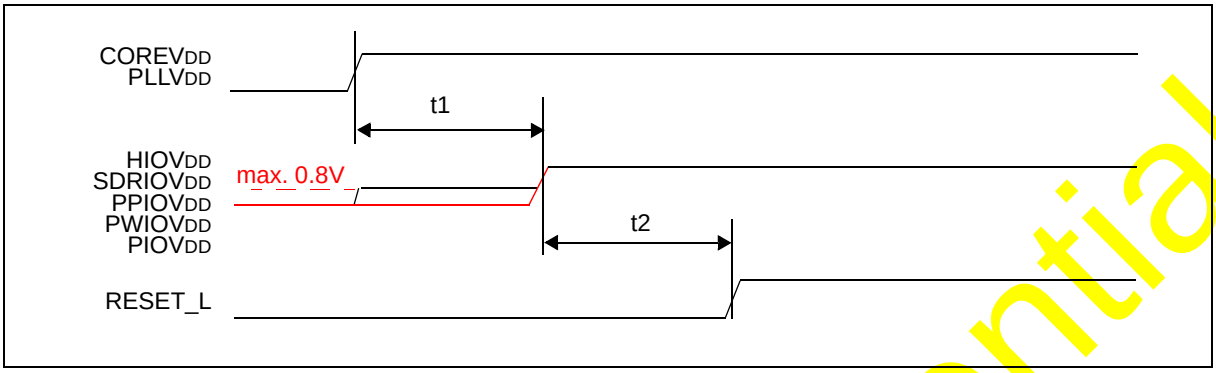


Figure 6-3: Power-On Sequence

Table 6-3: Power-On Sequence

Symbol	Parameter	Min	Max	Units
t1	HIOVDD, SDRIOVDD, PPIOVDD, PWIOVDD, PIOVDD on delay from COREVDD, PLLVDD on	0	500	ms
t2	RESET_L deasserted from HIOVDD, SDRIOVDD, PPIOVDD, PWIOVDD, PIOVDD on	50	—	ns

6.2.2 Power-Off Sequence

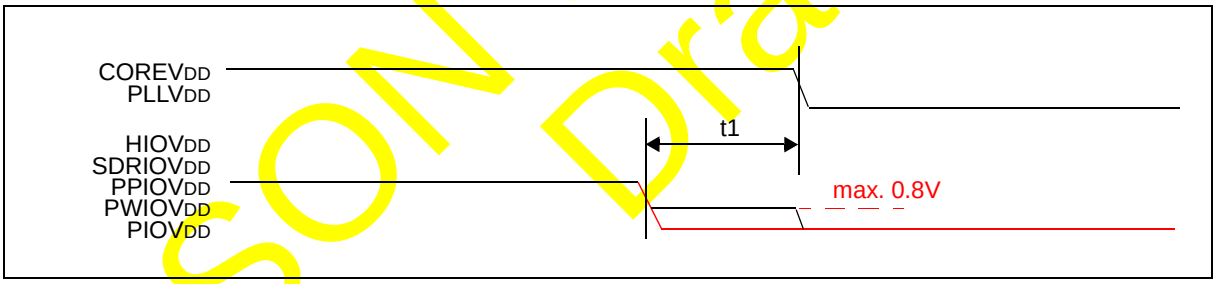


Figure 6-4: Power-Off Sequence

Table 6-4: Power-Off Sequence

Symbol	Parameter	Min	Max	Units
t1	COREVDD, PLLVDD off delay from HIOVDD, SDRIOVDD, PPIOVDD, PWIOVDD, PIOVDD off	0	500	ms

6.3 RESET_L Timing

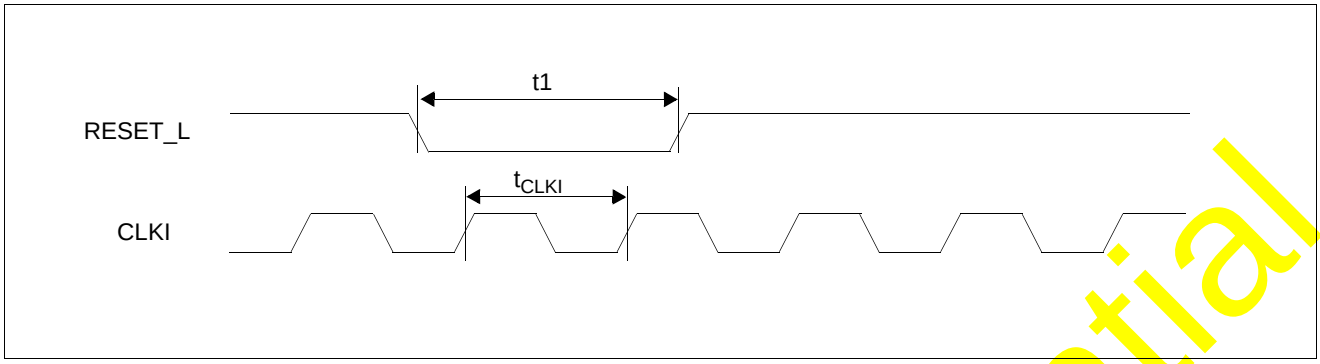


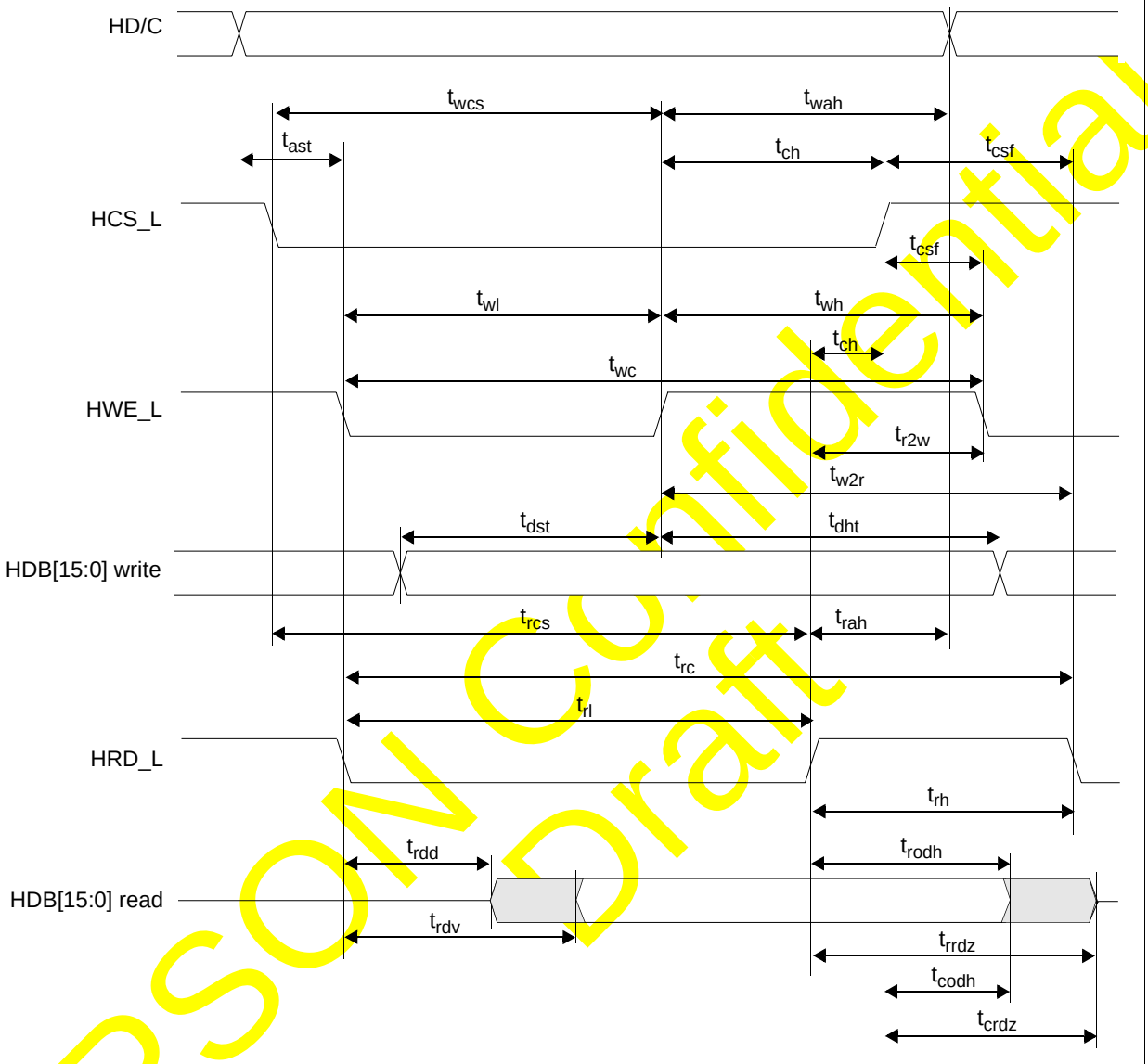
Figure 6-5 S1D13521 RESET_L Timing

Table 6-5 S1D13521 RESET_L Timing

Symbol	Parameter	Min	Max	Units
t1	Active Reset Pulse Width	1	—	CLKI

6.4 Host Interface Timing

6.4.1 16-bit Host Interface Timing



Note: The HD/C input pin is used to distinguish between Address and Data.

Note: The HCS_L pin can be kept low between write and read pulses as the register addresses will auto-increment. The register address will auto-increment in word increments for all register access except the Memory Data Port. Writes to the Memory Data Port will not increment the register address to support burst data writes to memory.

Figure 6-6: 16-bit Host Input A.C. Characteristics

Table 6-6: 16-bit Host Input A.C. Characteristics

Signal	Symbol	Parameter	Min	Max	Unit	Description
HD/C	t_{ast}	Address setup time (read/write)	1	—	ns	
	t_{wah}	Address hold time (write)	5	—	ns	
	t_{rah}	Address hold time (read)	29	—	ns	
HCS_L	t_{wcs}	Chip Select setup time (write)	t_{wl}	—	ns	
	t_{rcs}	Chip Select setup time (read)	t_{rl}	—	ns	
	t_{ch}	Chip Select hold time (read/write)	0	—	ns	
	t_{csf}	Chip Select Wait time (read/write)	1	—	ns	
HWE_L	t_{wl}	Pulse low duration	2	—	Ts	
	t_{wh}	Pulse high duration	1	—	Ts	
	t_{w2r}	HWE_L rising edge to HRD_L falling edge	2	—	Ts	
HRD_L	t_{r2w}	HRD_L rising edge to HWE_L falling edge	1	—	Ts	
	t_{rc}	Read cycle	$t_{rl} + t_{rh}$	—	ns	
	t_{rl}	Pulse low duration	5	—	Ts	
	t_{rh}	Pulse high duration for Registers	1	—	Ts	
		Pulse high duration for Memory and LUT	2	—	Ts	
HDB[15:0]	t_{dst}	Write data setup time	4	—	ns	
	t_{dht}	Write data hold time	7	—	ns	
	t_{rodh}	Read data hold time from HRD_L rising edge	11	—	ns	
	t_{rrdz}	HRD_L rising edge to HDB[15:0] Hi-Z	—	31	ns	
	t_{codh}	Read data hold time from HCS_L rising edge	1	—	ns	
	t_{crdz}	HCS_L rising edge to HDB[15:0] Hi-Z	—	8	ns	
	t_{rdv}	HRD_L falling edge to HDB[15:0] valid for Registers	—	16	ns	CL=30pF
		HRD_L falling edge to HDB[15:0] valid for Memory	—	5SYSCLK + 19	ns	
		HRD_L falling edge to HDB[15:0] valid for Registers	—	11	ns	CL = 8pF
		HRD_L falling edge to HDB[15:0] valid for Memory	—	5SYSCLK + 14	ns	
	t_{rdd}	HRD_L falling edge to HDB[15:0] driven	4	—	ns	CL=30pF
		HRD_L falling edge to HDB[15:0] driven	3	—	ns	CL = 8pF

1. Ts = System Clock period

6.5 Display Timings

The display frame settings are based on the display timing configuration registers as shown below.

Table 6-7: Display Timing Registers

Display Timing Name	Registers and Bits	Units
Frame Sync Length	(REG[0302h] bits 7-0) + 1	Lines
Frame Begin Length	REG[0304h] bits 7-0	Lines
Frame End Length	REG[0304h] bits 15-8	Lines
Frame Data Length	REG[0300h] bits 12-0	Lines
Line Sync Length	((REG[0308h] bits 7-0) x 4) + 2	Pixels
Line Begin Length	(REG[030Ah] bits 7-0) x 4	Pixels
Line End Length	(REG[030Ah] bits 15-8) x 4	Pixels
Line Data Length	REG[0306h] bits 12-0	Pixels

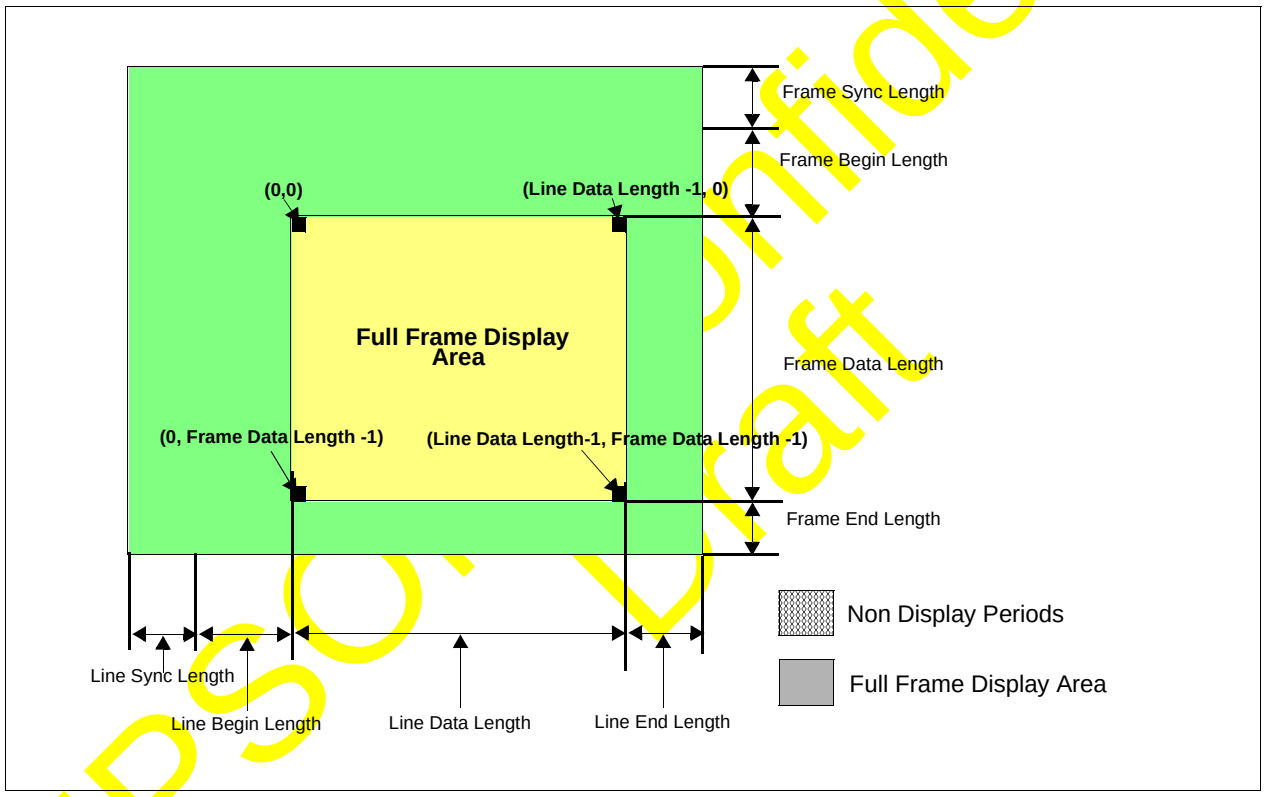


Figure 6-7: Display Timing

Note

To allow extra pixel lines to be hidden under the Line End Length, the display timing values should be programmed such that the following formula is valid.

(Line Data Length + Line End Length) ≥ Source Driver Output Total Count

6.5.1 Frame Rate Calculation Guide

The Frame Rate can be determined using the following formulas.

$$PixelClkFrequency = \frac{133Mhz}{PixelClkDivideSelected(REG[0018])}$$

$$SourceDriverClkFrequency = \frac{PixelClkFrequency}{PixelPerClockOutputSelect(REG[030C-Bit11])}$$

$$HorizontalTotalPixel = LineSyncLength + LineBeginLength + LineDataLength + LineEndLength$$

$$GateDriverGDCLKFrequency = \frac{SourceDriverClkFrequency}{HorizontalTotalPixel} MHz$$

$$VerticalTotalLines = FrameSyncLength + FrameBeginLength + FrameDataLength + FrameEndLength$$

$$FrameRate = \frac{GDCLKFrequency}{VerticalTotalLines}$$

The following shows example values for an 800x600 display.

Table 6-8 : Frame Rate Calculation Example for 800x600

Pixel Clock Divide Select	7	
Pixel Clock Frequency	16.625	MHz
SDCLK Frequency	8.3125	MHz

Internal Clock	133	MHz
Divide Selected	8	

Register Settings		
Frame Sync Length	4	
Frame Begin Length	4	
Frame End Length	5	
Frame Data Length	600	

Line Sync Length	10	
Line Begin Length	20	
Line End Length	40	
Line Data Length	800	

GDCLK High Time	230.5	SDCLKs
GDCLK Low Time	40	SDCLKs
GDCLK Frequency	30.73013	KHz

Total Lines	614	Lines
Frame Rate	50.04907	Hz

6.5.2 Interpreted Source Driver Timings

The following figure shows an example Source Driver connection using a Micronix MX860 (268 outputs per driver).

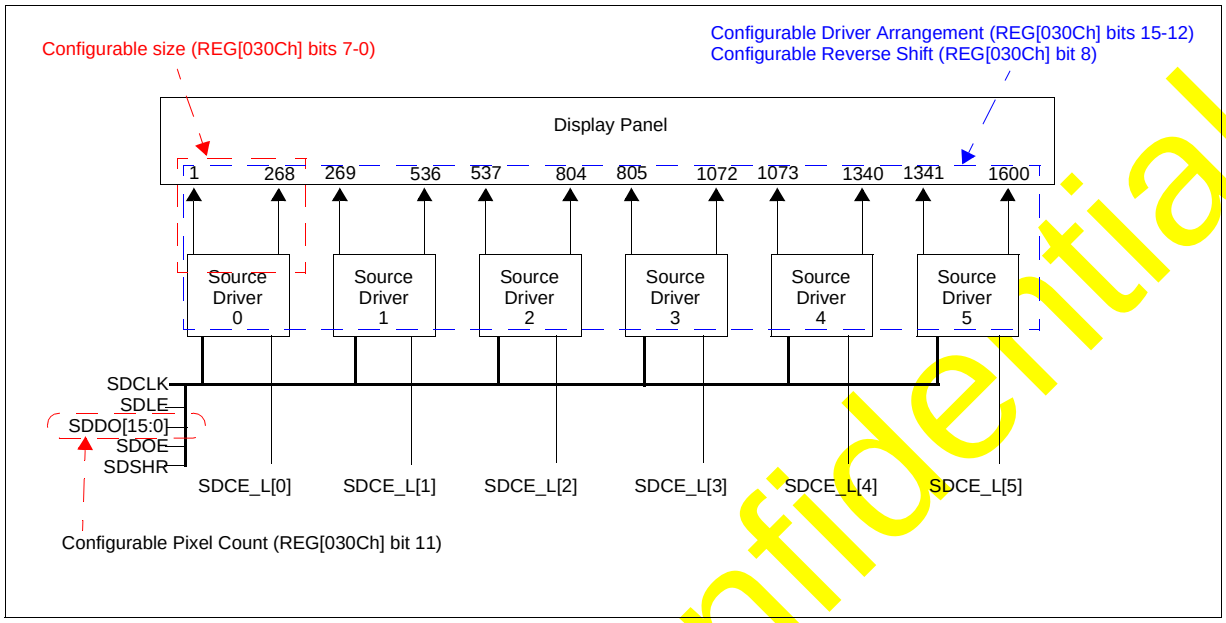


Figure 6-8: Source Driver Connection Example using MX860

Source Driver Display Timing 1: 4 Pixel per Clock Output

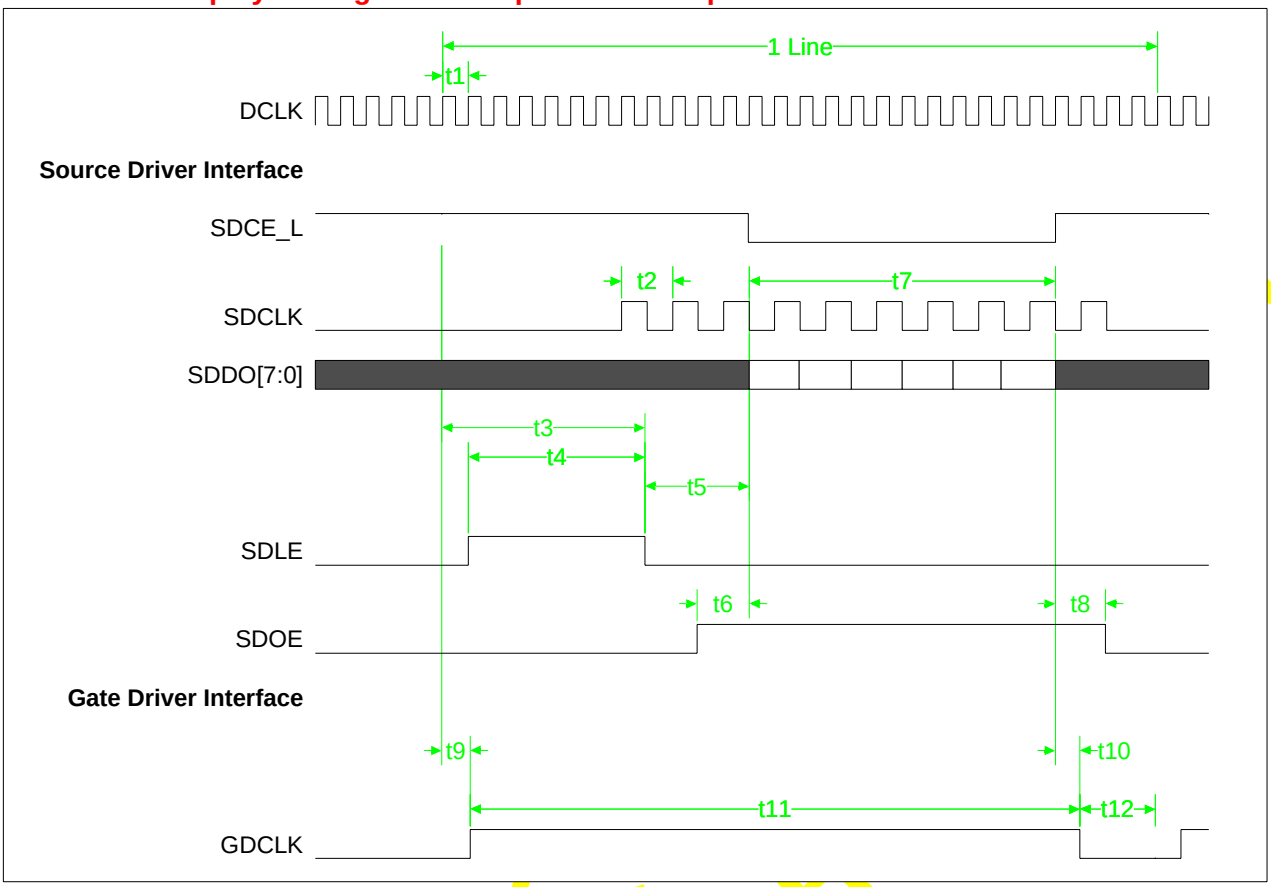


Figure 6-9: Source Driver Display Timing for 4 Pixel per clock Output

Table 6-9: Source Driver Display Timing for 4 Pixel Per Clock Output

Timing	Description	Value	Min	Max
t1	Dual Pixel Clock Period	From Pixel Clock Divide	12ns	—
t2	SDCLK Period for 4 Pixel per clock	2 x t1	24ns	—
t3	Line Start Length	(Line Start Length ÷ 4 x t2) + t1	3 x t1	—
t4	Source Driver Latch Enable High time	t3 - t1	t3 - t1	t3 - t1
t5	SDLE deassert to First Data output	(Line Begin Length ÷ 4 x t2)	0	—
t6	Source Driver Output Enable before Data Valid	1 x t2	1 x t2	1 x t2
t7	Data Output Time	Line Data Length ÷ 4 x t2	2 x t2	—
t8	SDOE deassert time from last data output	(Line End Length ÷ 4 x t2) - t1	1 x t2	—
t9	Gate Driver Clock positive edge	1 x t1	1 x t1	1 x t1
t10	Gate Driver Clock negative edge	1 x t1	1 x t1	1 x t1
t11	Gate Driver Clock High Time	((Line Start + Line Begin + Line Data Length) ÷ 4 x t2) + t10	1 x t2	—
t12	Gate Driver Clock Low Time	(Line End Length ÷ 4 x t2) - t10	1 x t2	—

Source Driver Display Timing 2: 8 Pixel per Clock Output

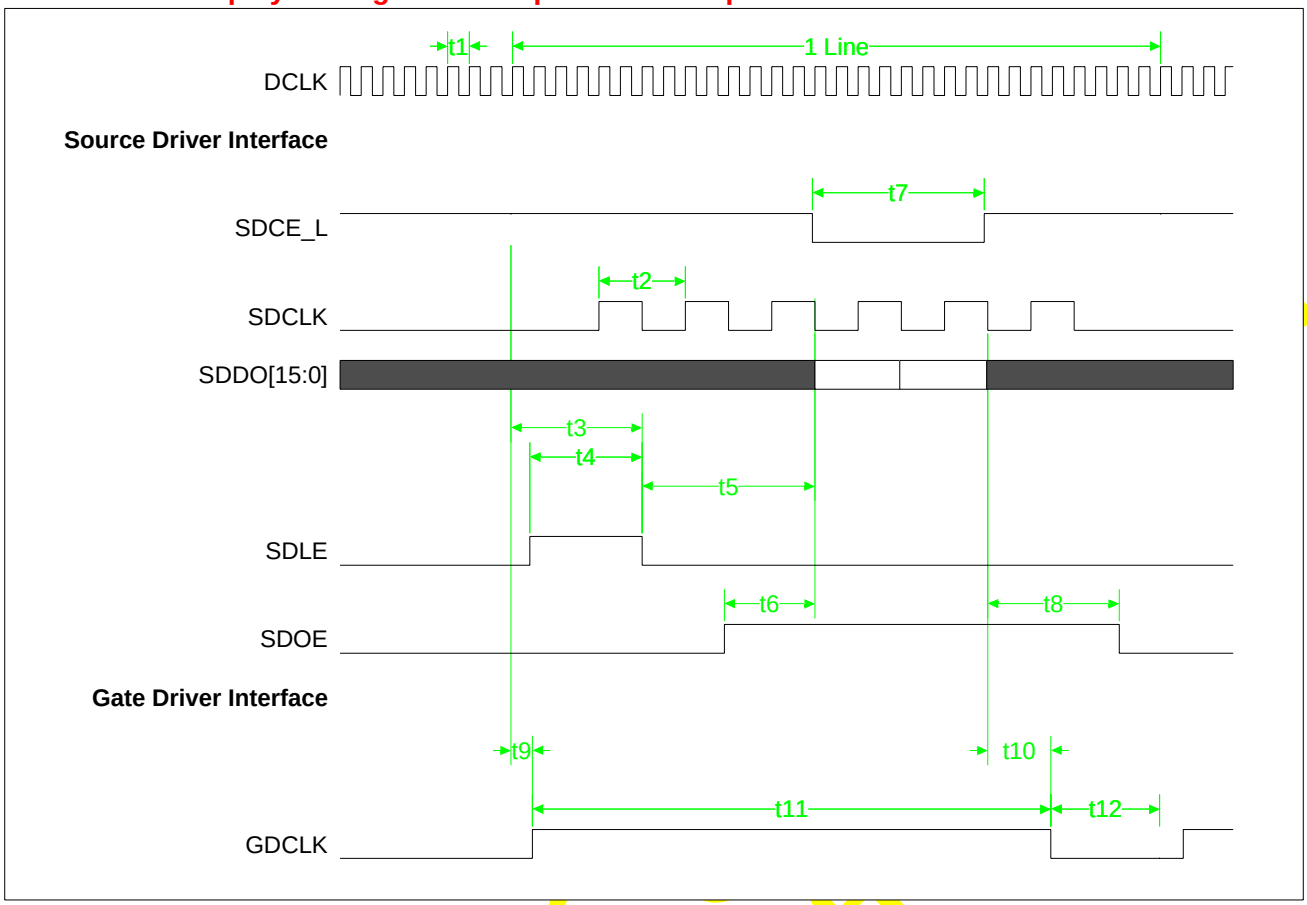


Figure 6-10: Source Driver Display Timing for 8 Pixel per clock Output

Table 6-10: Source Driver Display Timing for 8 Pixel Per Clock Output

Timing	Description	Value	Min	Max
t1	Dual Pixel Clock Period	From Pixel Clock Divide	12ns	—
t2	SDCLK Period for 8 Pixel per clock	4 x t1	48ns	—
t3	Line Start Length	(Line Start Length ÷ 8 x t2) + t1	3 x t1	—
t4	Source Driver Latch Enable High time	t3 - t1	t3 - t1	t3 - t1
t5	SDLE deassert to First Data output	(Line Begin Length ÷ 8 x t2)	0	—
t6	Source Driver Output Enable before Data Valid	1 x t2	1 x t2	1 x t2
t7	Data Output Time	Line Data Length ÷ 8 x t2	2 x t2	—
t8	SDOE deassert time from last data output	(Line End Length ÷ 8 x t2) - t2	1 x t2	—
t9	Gate Driver Clock positive edge	1 x t1	1 x t1	1 x t1
t10	Gate Driver Clock negative edge	3 x t1	3 x t1	3 x t1
t11	Gate Driver Clock High Time	((Line Start + Line Begin + Line Data Length) ÷ 8 x t2) + t10	1 x t2	—
t12	Gate Driver Clock Low Time	(Line End Length ÷ 8 x t2) - t10	1 x t2	—

Source Driver Display Timing 3: 4 Pixel per Clock Edge Output (Double Data Rate)

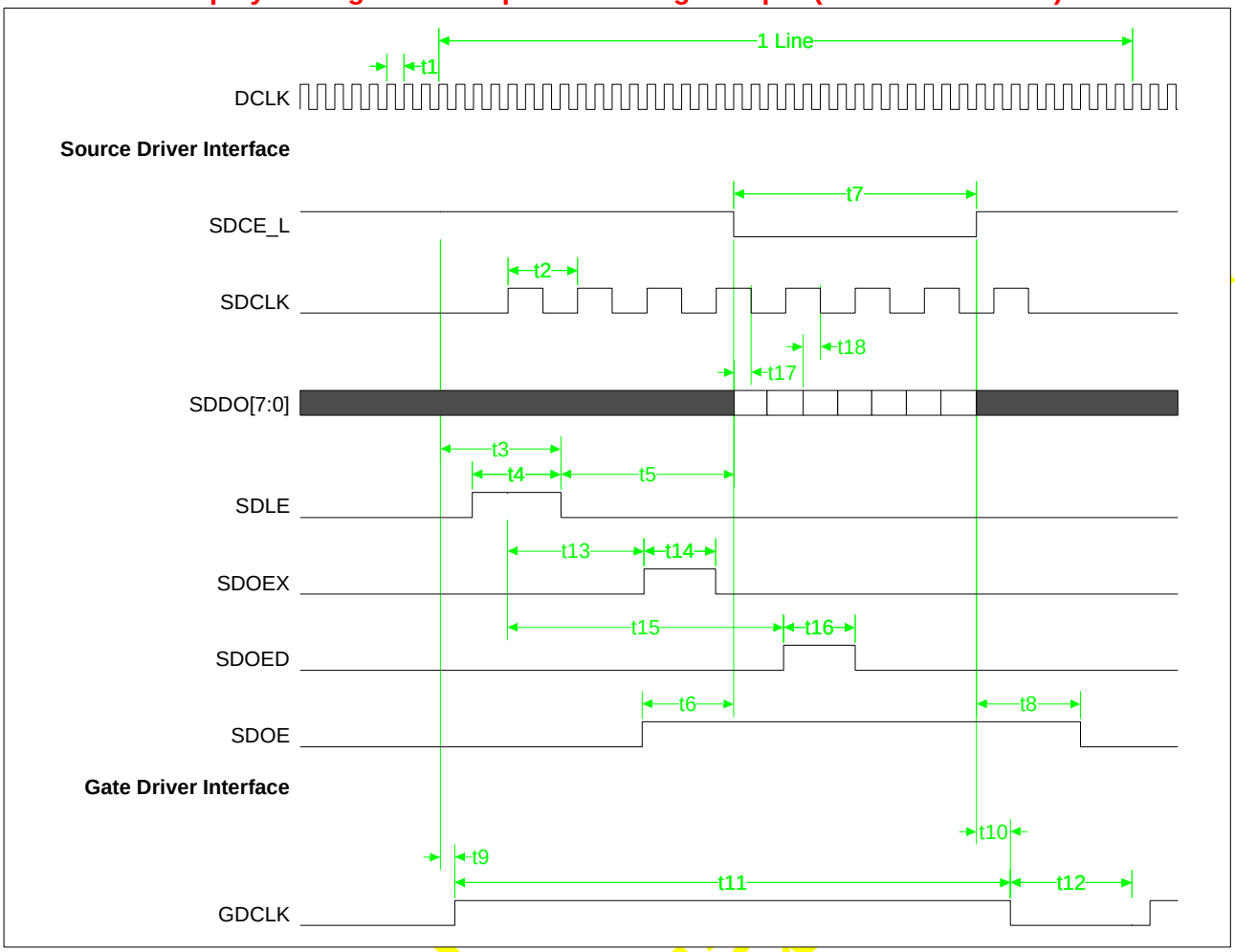


Figure 6-11: Source Driver Display Timing for 4 Pixel per Clock Edge Output

Table 6-11: Source Driver Display Timing for 4 Pixel per Clock Edge Output

Timing	Description	Value	Min	Max
t1	Dual Pixel Clock Period	From Pixel Clock Divide	12ns	—
t2	SDCLK Period for 8 Pixel per clock	4 x t1	48ns	—
t3	Line Start Length	(Line Start Length ÷ 8 x t2) + t1	3 x t1	—
t4	Source Driver Latch Enable High time	t3 - (2 x t1)	t3 - (2 x t1)	t3 - (2 x t1)
t5	SDLE deassert to First Data output	(Line Begin Length ÷ 8 x t2)	0	—
t6	Source Driver Output Enable before Data Valid	t2 + t1	t2 + t1	t2 + t1
t7	Data Output Time	Line Data Length ÷ 8 x t2	2 x t2	—
t8	SDOE deassert time from last data output	(Line End Length ÷ 8 x t2) - t2	1 x t2	—
t9	Gate Driver Clock positive edge	1 x t1	1 x t1	1 x t1
t10	Gate Driver Clock negative edge	2 x t1	2 x t1	2 x t1
t11	Gate Driver Clock High Time	((Line Start + Line Begin + Line Data Length) ÷ 8 x t2) + t10	1 x t2	—
t12	Gate Driver Clock Low Time	(Line End Length ÷ 8 x t2) - t10	1 x t2	—
t13	SDOEX assert Delay	((REG[030Eh] bits 7-3) x t2)	1 x t2	—
t14	SDOEX Pulse Width	1 x t2	1 x t2	1 x t2
t15	SDOED assert Delay	((REG[030Eh] bits 15-11) x t2)	1 x t2	—
t16	SDOED Pulse Width	1 x t2	1 x t2	1 x t2
t17	Data Output Setup Time to SDCLK Edge	1 x t1	1 x t1	1 x t1
t18	Data Output Hold Time to SDCLK Edge	1 x t1	1 x t1	1 x t1

6.5.3 Interpreted Gate Driver Timings

The following figure shows an example Gate Driver connection using a Sharp LH1692.

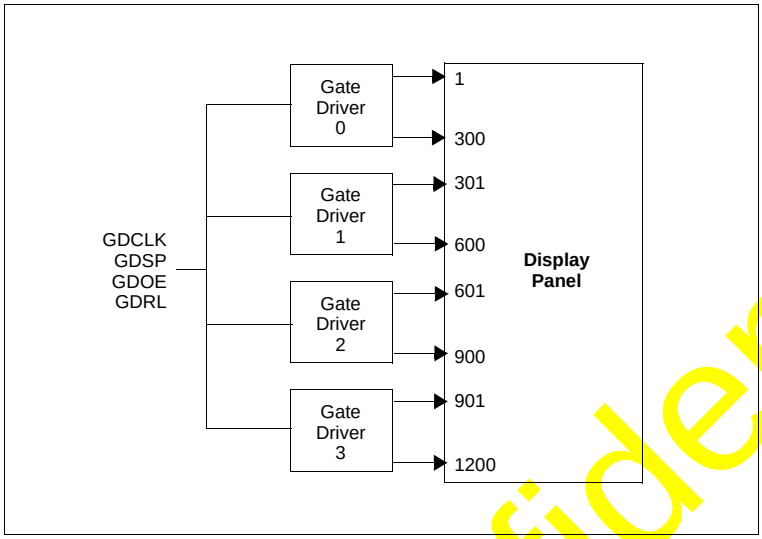


Figure 6-12: Gate Driver Connection Example using Sharp LH1692

Gate driver timings are separated into 2 sections:

- GDCLK: GDCLK is generated from Line Clock (LCLK) and Pixel Data Enable (PDEN). GDCLK is used by the gate drivers to enable gate data output.
- GDSP: GDSP is generated from GDCLK to signal a start pulse.

Gate Driver Display Timings

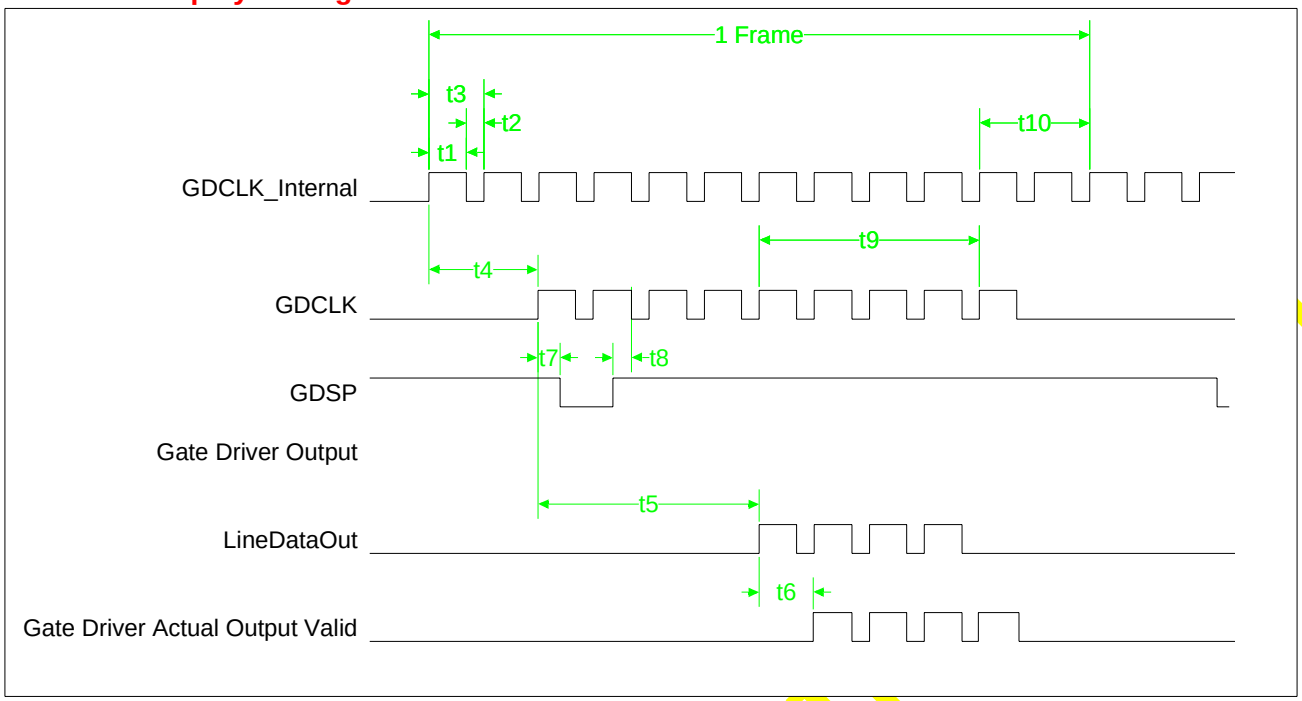


Figure 6-13: Gate Driver Timing Generation

Table 6-12: Gate Driver Timing Generation

Timing	Description	Value	Min	Max
t1	GDCLK High Level	Line Start + Line Begin + Line Data Length	4 x DClk	—
t2	GDCLK Low Level	Line End Length	4 x DClk	—
t3	1 Line Width	t1 + t2	~	—
t4	Frame Sync Length	Frame Sync Length x t3	2 x t3	—
t5	Frame Begin Length	Frame Begin Length x t3	0	—
t6	Gate Driver's Actual output Valid	Fixed Timing	1 x t3	1 x t3
t7	GDCLK to GDSP negative edge	t1 ÷ 2	t1 ÷ 2	t1 ÷ 2
t8	GDCLK to GDSP positive edge\	t1 ÷ 2	t1 ÷ 2	t1 ÷ 2
t9	Frame Data Length	Frame Data Length x t3	1 x t3	—
t10	Frame End Length	Frame End Length x t3	1 x t3	—

6.6 Power Pin Interface

6.6.1 Power Pin Transition Sequence for PWR[3:0]

The power pins PWR[3:0] operate in a cascade manner with the delay times controlled by register settings (REG[0234h] ~ REG[0238h]).

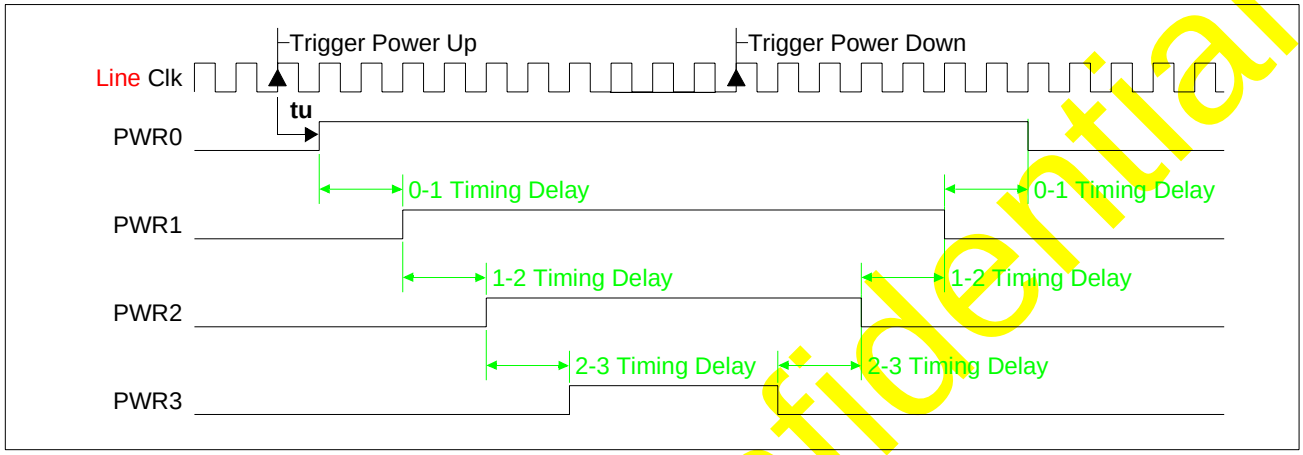


Figure 6-14: PWR[3:0] Transition Sequence

Table 6-13: PWR[3:0] Transition Timing

Symbol	Parameter	Min	Max	Units
tu	Trigger Power up to Power Pin 0 transition	0	—	ns
0-1 Timing Delay	Power pin 0 to Power pin 1 Timing Delay	1	REG[0234h]	Line Clk
1-2 Timing Delay	Power pin 1 to Power pin 2 Timing Delay	1	REG[0236h]	Line Clk
2-3 Timing Delay	Power pin 2 to Power pin 3 Timing Delay	1	REG[0238h]	Line Clk

6.6.2 Power Pin Transition Sequence for PWRCOM

The power pin PWRCOM defines the common power control. PWRCOM operations are controlled by the Display Engine update operation as shown in the following figure.

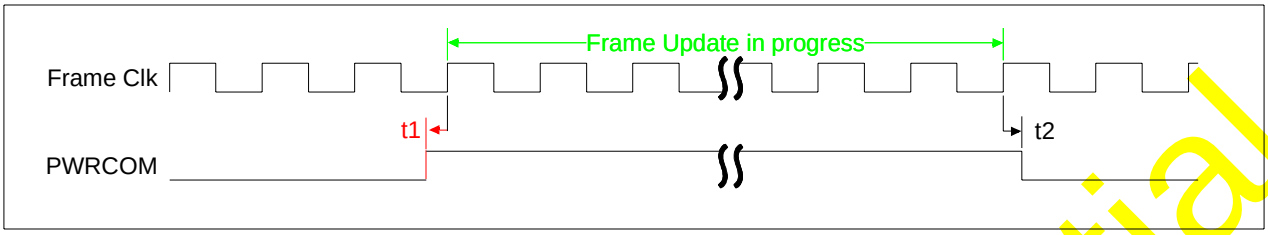


Figure 6-15: PWRCOM Transition Sequence

Table 6-14: PWRCOM Transition Timing

Symbol	Parameter	Min	Max	Units
t1	PWRCOM Active to Frame Clk	0	—	ns
t2	Frame Clk to PWRCOM Inactive	0	—	ns

Chapter 7 Clocks

7.1 Clock Descriptions

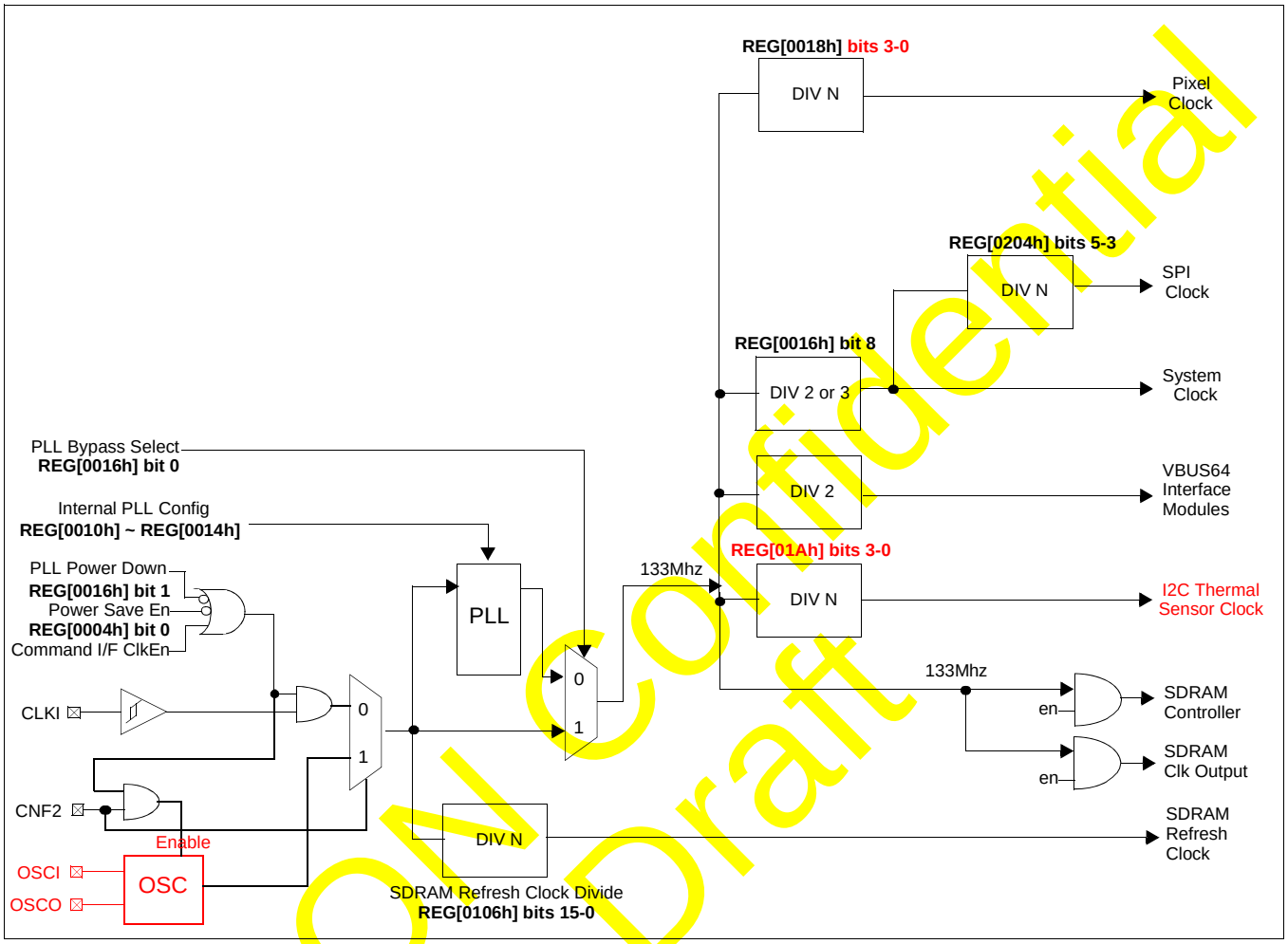


Figure 7-1: Clock Tree Diagram

Chapter 8 Power Management

8.1 Power Management State Description

The S1D13521 controller has the following power states:

- OFF State: Power for the S1D13521 and external SDRAM is off.
- Run State: Normal Operation for the S1D13521. The display can be updated.
- Standby State: S1D13521 is in power save mode and SDRAM is in a Self Refresh state.
- Sleep Mode: S1D13521 is in power save mode and SDRAM is in Self Refresh state. Initiates the Power Pins power down cycles.

The following table summarizes the S1D13521 controller and SDRAM states.

Table 8-1: S1D13521 Controller and SDRAM States

Power Mode	S1D13521 Controller State	S1D13521 PLL State	SDRAM State	SDRAM Data Retained
OFF	Unknown	Unknown	Unknown	No
Run	Active All clocks active	Active	Normal Operation with Auto Refresh	Yes
Standby	Power Save Mode All module clocks gated off PLL is running	Active	Self Refresh	Yes
Sleep	Power Save Mode Power Pin cycle off PLL off	Powered-Down	Self Refresh	Yes

Table 8-2: State Transition Requirements

	Next State Requirements			
Current State	**OFF**	**Run**	**Standby**	**Sleep**
OFF	NA	1. Reset 2. Init PLL (Wait 200µs) 3. Init SDRAM (Wait 100µs) 4. Ready for operation	Not Possible. Must Reset to Run State	Not Possible. Must Reset to Run State
Run	1. Host Save Memory Contents 2. Turn off Power	NA	1. Issue Standby	1. Host Issue Run 2. SDRAM Self Refresh 3. Issue Sleep 4. Power-Pin seq 5. Turn off PLL
Standby	1. Host issue Run 2. Host Save Memory Contents 3. Turn off Power	1. Issue Run 2. SDRAM exit Self Refresh 3. Ready for Operation	NA	1. Issue Run 2. Issue Sleep 3. Power-Pin Seq 5. Turn Off PLL
Sleep	1. Turn off Power	1. Issue Run 2. Init PLL (Wait 200µs) 3. SDRAM exit Self Refresh 4. Power-Pin Seq 5. Ready for Operation	1. Host Issue Run 2. Power-Pin Seq 3. Issue standby	NA

Transitioning to any Power State is only possible from the RUN state.

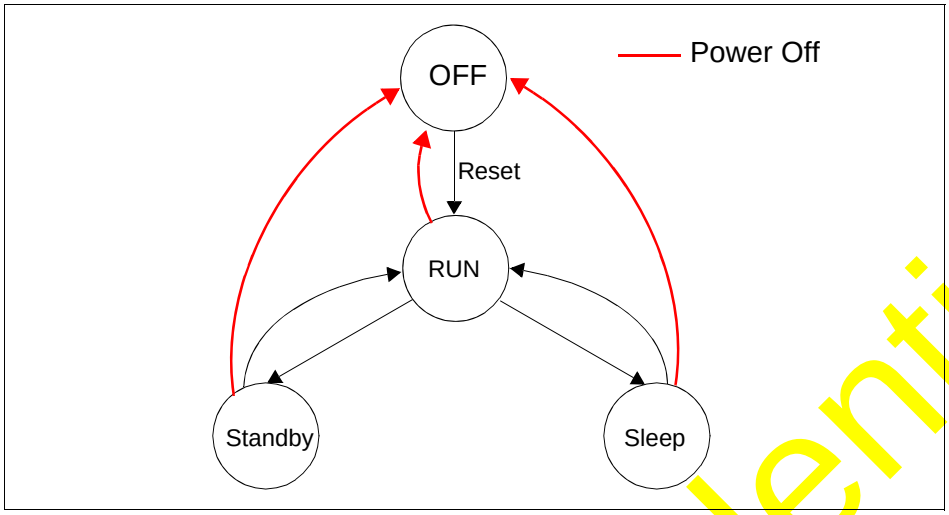


Figure 8-1: State Transition Diagram

Chapter 9 Host Interface

9.1 Host Cycle Sequences

9.1.1 Command and Parameter Cycle

A typical cycle consists of a Command and a variable number of parameters depending on the expected parameter count for each specific command. The following figures shows a typical cycle.

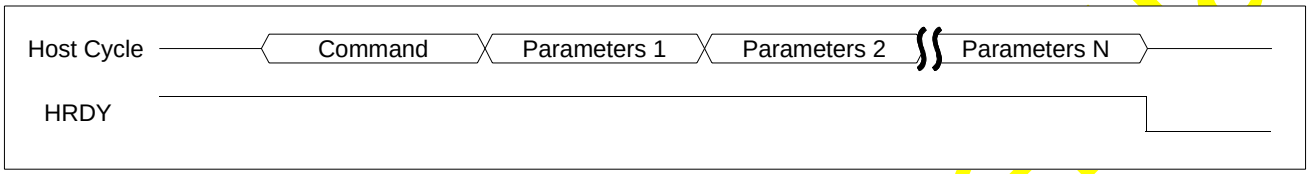


Figure 9-1: Command Mode Host Cycle Example

The HRDY line is deasserted (low) within 5ns after the last parameter. When the sequencer is ready to accept new commands, HRDY is asserted (high) again.

9.1.2 Memory Access Combination Cycle

Commands that require Host memory access require a combination of Command/Parameter and Register Read/Write cycles. The HRDY line will deassert (low) during the memory read/write data cycles.

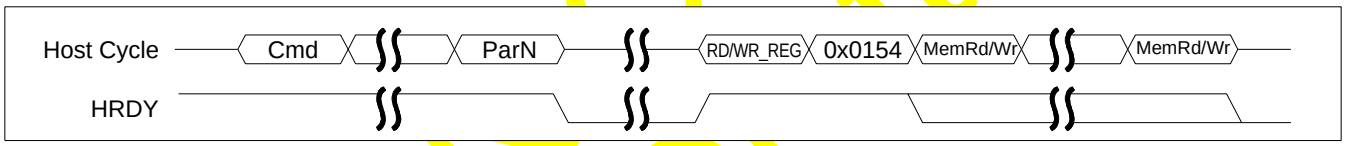


Figure 9-2: Memory Access Combination Cycle

9.2 HRDY (Wait Line) Usage

When a command is issued, the command sequencer must execute a set of instruction codes based on the specific command. The execution time required for each command depends on the number of instruction codes that must be completed.

Once a command is issued, the host interface must not issue any new commands until HRDY is asserted High. If the HRDY line is not used, the Host can poll the Sequence Controller Busy Status bit in REG[000Ah] using the RD_REG command.

Note
RD_REG is implemented outside of the Sequence Controller and is specifically designed to allow execution in parallel with other command sequences. This is useful for polling the Sequence Controller Busy Status by Hosts that do not have HRDY.

The following figure shows a typical command/parameter sequence using Sequence Controller Busy Status polling.

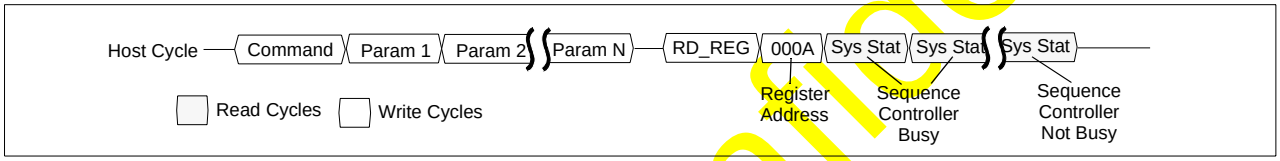


Figure 9-3: Command Mode Host Cycle Example for Host without HRDY

9.3 Command Operation

The following figure shows a typical command mode operation with parameter/data writes only.

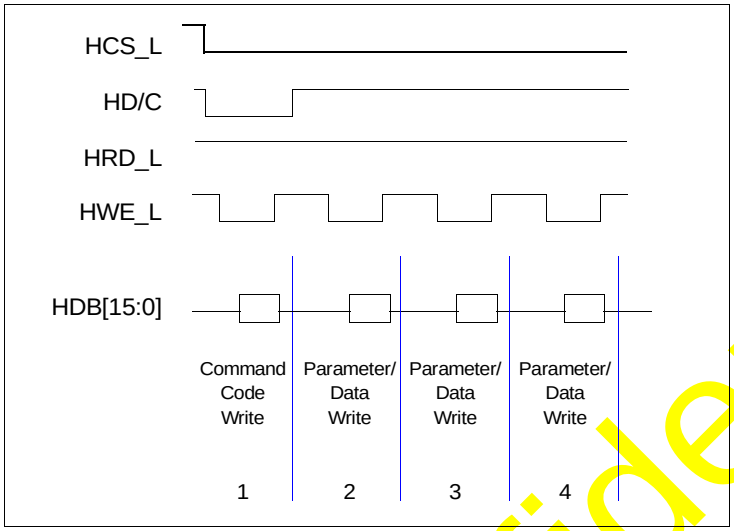


Figure 9-4: Command Mode Operation - Parameter/Data Writes Only

The following figure shows a typical command mode operation for reading register data.

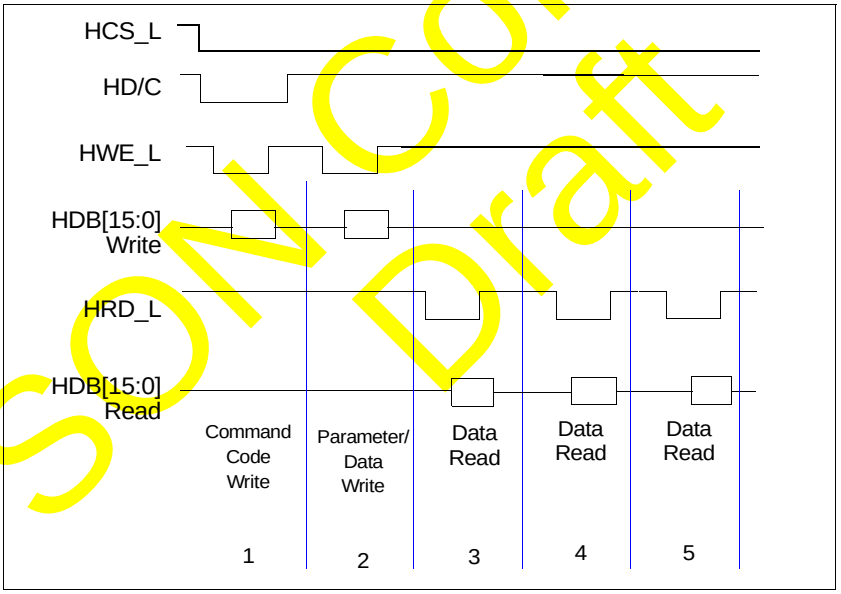


Figure 9-5: Command Mode Operation - Register Read Data

9.4 Command List

The following commands are applicable for the 16-bit Indirect Interface.

Table 9-1: Host Interface Command Summary

Code 16-bit Indirect - 2 bytes	Command	Parameters					Description
		1	2	3	4	5	
System Commands							
0x00	INIT_CMD_SET	SPI Config	SFM Adr[15:0]	SFM[23:16]	—	—	Initialize Instruction code from Specific Serial Flash Address
0x01	INIT_PLL_STBY	PLL Config0	PLL Config1	PLL Config2	—	—	Initialize PLL and Go Into Standby Mode
0x02	RUN_SYS	—	—	—	—	—	Run System using PLL
0x04	STBY	—	—	—	—	—	Go to Standby Mode
0x05	SLP	—	—	—	—	—	Go to Sleep Mode
0x06	INIT_SYS_RUN	—	—	—	—	—	Initialize System and Go into Run State
0x07	INIT_SYS_STBY	—	—	—	—	—	Initialize System and Go into Standby State
0x08	INIT_SDRAM	SDRAMCFG0	SDRAMCFG1	SDRAMCFG2	SDRAMCFG3	—	Initialize SDRAM
0x09	INIT_DSPE_CFG	HSIZE	VSIZE	SDRVCFG	GDRVCFG	LUT Index Format CFG	Initialize Display Engine
0x0A	INIT_DSPE_TMG	Frame Sync CFG	Frame Begin/End CFG	Line Sync CFG	Line Begin/End CFG	Pixel Clock CFG	Initialize Driver Timings
0x0B	INIT_ROTMODE	ROTMODE	—	—	—	—	Initialize Rotation Mode Timings
Register and Memory Access Commands							
0x10	RD_REG	REGADDR[15:0]	RDATA[15:0]	—	—	—	Read Register **Refer to detailed descriptions**
0x11	WR_REG	REGADDR[15:0]	WDATA[15:0]	—	—	—	Write Register **Refer to detailed descriptions**
0x12	RD_SFM	—	—	—	—	—	Trigger Serial Flash Read Operation
0x13	WR_SFM	WDATA[15:0]	—	—	—	—	Trigger Serial Flash Write Operation
0x14	END_SFM	—	—	—	—	—	END SFM Operation
Burst Access Commands							
0x1C	BST_RD_SDR	MA[15:0]	MA[31:16]	BC[15:0]	BC[31:16]	—	Start Burst Read SDRAM Memory
0x1D	BST_WR_SDR	MA[15:0]	MA[31:16]	BC[15:0]	BC[31:16]	—	Start Burst Write SDRAM Memory
0x1E	BST_END_SDR	—	—	—	—	—	Burst End
Image Loading Commands							
0x20	LD_IMG	ARG[15:0]	—	—	—	—	Load Image Full
0x22	LD_IMG_AREA	ARG[15:0]	XSTART[15:0]	YSTART[15:0]	WIDTH[15:0]	HEIGHT[15:0,	Load Image Area With parameters
0x23	LD_IMG_END	—	—	—	—	—	Load Image End
0x24	LD_IMG_WAIT	—	—	—	—	—	Load Image Wait End
0x25	LD_IMG_SETADR	MA[15:0]	MA[31:16]	—	—	—	Set Load Image Manual Address
0x26	LD_IMG_DSPEADR	—	—	—	—	—	Set Load Image to use Display Engine's Address
Polling Commands							
0x28	WAIT_DSPE_TRG	—	—	—	—	—	Wait For Display Engine Trigger Done
0x29	WAIT_DSPE_FREND	—	—	—	—	—	Wait For Display Engine Frame End
0x2A	WAIT_DSPE_LUTFREE	—	—	—	—	—	Wait For Display Engine At least 1 LUT is Free
0x2B	WAIT_DSPE_MLUTFREE	LUT Mask [15:0]	—	—	—	—	Wait For Display Engine At least 1 Masked LUT is Free

Table 9-1: Host Interface Command Summary

Code 16-bit Indirect - 2 bytes	Command	Parameters					Description
		1	2	3	4	5	
Waveform Update Commands							
0x30	RD_WFM_INFO	MA[15:0]	MA[31:16]	—	—	—	Read Waveform Information
0x32	UPD_INIT	—	—	—	—	—	Update Buffer Initialize
0x33	UPD_FULL	ARG[15:0]	—	—	—	—	Update Buffer Full
0x34	UPD_FULL_AREA	ARG[15:0]	XSTART[15:0]	YSTART[15:0]	WIDTH[15:0]	HEIGHT[15:0]	Update Buffer Full Area
0x35	UPD_PART	ARG[15:0]	—	—	—	—	Update Buffer Partial
0x36	UPD_PART_AREA	ARG[15:0]	XSTART[15:0]	YSTART[15:0]	WIDTH[15:0]	HEIGHT[15:0]	Update Buffer Partial Area
0x37	UPD_GDRV_CLR	—	—	—	—	—	Gate Driver Clear Command
0x38	UPD_SET_IMGADR	ADR[15:0]	ADR[31:16]	—	—	—	Set Image Buffer Start Address
0x38-0x3F	**Reserved**	—	—	—	—	—	Reserved

9.5 Host Interface Command Descriptions

The Command Sequencer supports up to 64 available commands. The first 8 commands (command codes 0x00 ~ 0x07) turn on the temporary clock enable until the command sequence has finished. This feature is for implementing commands (i.e. INIT_CMD_SET, INIT_PLL, SLP) where the S1D13521 is, or will be, in SLP mode before or after the command sequence command is completed. In SLP mode, the input clock is gated off in order to minimize power consumption. However, a clock is needed for the Sequencer Controller logic while it is operating.

Three commands are reserved and cannot be re-programmed.

- 0x00 - INIT_CMD_SET
- 0x10 - RD_REG
- 0x11 - WR_REG

These commands are hard-coded in logic allowing them to operate even before the pre-programmed command sequence is loaded into the chip. RD_REG (which can be executed in parallel with the Sequence Controller) can poll the busy status of the Sequence Controller to determine when the previous command sequence has finished. This is useful for Hosts that have no HRDY support.

Note
Although the RD_REG and WR_REG commands can be executed in parallel with the Sequence Controller, register reads/writes are not recommended while the Sequence Controller is in operation. The exception to this rule is polling the busy status bit.

9.5.1 INIT_CMD_SET (0x00 + 3 parameters)

This command initializes the Command Interface instruction table and codes. The parameters setup the SPI operating mode and the Serial Flash Memory address where the instruction table and codes are stored.

Parameter Count = 3

Parameter 1 (Recommended Setting = 0x0041)

n/a							
15	14	13	12	11	10	9	8
SPI Flash Access Mode Select	SPI Flash Read Command Select	SPI Flash Clock Divide Select bits 2-0			SPI Flash Clock Phase Select	SPI Flash Clock Polarity Select	SPI Flash Enable
7	6	5	4	3	2	1	0

bit 7 SPI Flash Access Mode Select
This bit selects between Display Engine access mode and Host Register access mode. This bit must be set to 1b before performing a Display Engine operation to allow the Display Engine to communicate with SPI Flash Memory.
When this bit = 0b, Host Register access mode is selected.
When this bit = 1b, Display Engine access mode is selected.

bit 6 SPI Flash Read Command Select

This bit selects which serial flash command is used for reading data and depends on the SPI Flash Memory device. Refer to the device data sheet to determine the appropriate setting.

When this bit = 0b, the serial flash read speed is Low.

When this bit = 1b, the serial flash read speed is High.

bits 5-3 SPI Flash Clock Divide Select bits [2:0]

These bits select the divide ratio for the SPI Flash Clock which is derived from either the PLL output or CLKI depending on the setting of the PLL Bypass Mode Enable bit, REG[0016h] bit 0. For further details on the clock structure, see Section Chapter 7, “Clocks” on page 45.

Table 9-2: SPI Flash Clock Divide Ratio Selection

bits 5-3	SPI Flash Clock Divide Ratio	bits 5-3	SPI Flash Clock Divide Ratio
000b	1:2	100b	1:6
001b	1:3	101b	1:7
010b	1:4	110b	1:8
011b	1:5	111b	1:9

bit 2 SPI Flash Clock Phase Select

This bit selects the SPI Flash clock phase. For a summary of the SPI Flash Memory clock phase and polarity settings, see Table 10-19 “SPI Flash Clock Phase and Polarity,” on page 100.

bit 1 SPI Flash Clock Polarity Select (CPOL)

This bit selects the SPI Flash clock polarity. The following table summarizes the SPI Flash clock polarity and phase settings.

Table 9-3 : SPI Flash Clock Phase and Polarity

bit 2	bit 1	Valid Data	Clock Idling Status
0b	0b	Rising edge of SPI Flash Clock	Low
	1b	Falling edge of SPI Flash Clock	High
1b	0b	Falling edge of SPI Flash Clock	Low
	1b	Rising edge of SPI Flash Clock	High

bit 0 SPI Flash Enable

This bit controls the SPI Flash Memory interface logic.

When this bit = 0b, the SPI Flash Memory interface is disabled.

When this bit = 1b, the SPI Flash Memory interface is enabled.

Note

The SPI Flash Memory interface should be disabled (REG[0204h] bit 0 = 0b) before programming the SPI Flash registers, REG[0200h] ~ REG[0208h].

Parameter 2							
Serial Flash Memory Address Select bits 15-8							
15	14	13	12	11	10	9	8
Serial Flash Memory Address Select bits 7-0							
7	6	5	4	3	2	0	0

Parameter 3							
15	14	13	12	11	10	9	8
Serial Flash Memory Address Select bits 23-16							
7	6	5	4	3	2	0	0

Parameter 3 bits 7-0
Parameter 2 bits 15-0 Serial Flash Memory Address Select bits [23:0]
These bits specify the memory start address in the Serial Flash Memory where the Instruction Codes are located.

9.5.2 INIT_PLL_STBY (0x01 + 3 parameters)

This command initializes the PLL and sets the S1D13521 into Standby Mode. PLL Configuration is programmed using the three input parameters. When PLL Lock is asserted, this command sequence is completed.

Functions performed:
1. Program PLL registers
2. Disable PLL Power Down (REG[0016h]) to 0001h
3. Wait for PLL Lock
4. Program State Status register to Standby Mode (REG[000Ah] bits 12-10 = 2h)
5. Turn On Power Save Mode (REG[0006h] bit 0 = 1b)

Next Command Blocking: Yes

Parameter 1							
PLL Setting 0 bits 7-0							
15	14	13	12	11	10	9	8
n/a		M-Divider bits 5-0					
7	6	5	4	3	2	1	0

bits 15-8 PLL Setting 0 bits [7:0]
These bits must be set to F8h.

bits 5-0 M-Divider bits [5:0]

These bits determine the divide ratio between CLKI and the actual input clock to the PLL. These bits must be set such that the internal input clock to the PLL (PLLCLK) is between 1MHz and 2MHz.

Table 9-4: PLL M-Divide Selection

bits 5-0	M-Divider Ratio
0h	1:1
01h	2:1
02h	3:1
03h	4:1
• • •	• • •
20h	33:1
21h to 3Fh	Reserved

Parameter 2

PLL Setting 1 bits 15-8							
15	14	13	12	11	10	9	8
PLL Setting 1 bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 PLL Setting 1 bits [15:0]

These bits must be set to 2880h.

Parameter 3							
n/a	L-Counter bits 6-0						
15	14	13	12	11	10	9	8
PLL Setting 2 bits 7-0							
7	6	5	4	3	2	1	0

bits 14-8 L-Counter bits [6:0]

These bits are used to configure the PLL Output (in MHz) and must be set according to the following formula.

PLL Output = (L-Counter + 1) x PLLCLK
= LL x PLLCLK

Where:

PLL Output is the desired PLL output frequency (in MHz).
L-Counter is the value of this register (in decimal).
PLLCLK is the internal input clock to the PLL (in MHz).

Table 9-5 PLL Setting Example

Target Frequency (MHz)	LL	CLKI Input Clock (MHz)	M-Divider (bits 5-0)	M-Divide Ratio	PLLCLK (MHz)	POUT (MHz)
133	110	12	09h	10:1	1.2	132

bits 7-0 PLL Setting 2 bits [7:0]

These bits must be set to 00h.

9.5.3 RUN_SYS (0x02 + 0 parameters)

This command places the S1D13521 into normal operation mode. This includes enabling the PLL and/or disabling power save mode (i.e. removing the S1D13521 from Standby or Sleep mode).

Functions performed:
1. Disable PLL Power Down (if not disabled already)
2. Wait for PLL Lock (if step 1 is valid)
3. Disable Power Save Mode (REG[0006h] bit 0 <= 0)
4. Trigger Power Pin - On Sequence
5. Trigger SDRAM - Exit Self-Refresh
6. Wait for SDRAM - Ensure Self-Refresh is exited and Power Pin sequence is done
7. Program State Status Register (REG[000Ah] bits 12-10 to 1h (Normal Operation)

Next Command Blocking: Yes

9.5.4 STBY (0x04 + 0 parameters)

This command places the S1D13521 into Standby mode. To wake up from Standby mode, use the RUN_SYS command.

Functions performed:
1. Wait for all modules to be idle (HMEM, I2C, SPI, PWR, 3-wire, SDRAM, and DSPE)
2. Power Pin (Enter Off State)
3. SDRAM (Enter Self-Refresh Mode)
4. SDRAM (Wait for Self-Refresh Mode Entered) and Power Pin (Wait for Off State Entered)
5. Program State Status register to Standby Mode (REG[000Ah] bits 12-10 = 2h)
6. Power Save (Enable)

Next Command Blocking: Yes

9.5.5 SLP (0x05 + 0 parameters)

This command places the S1D13521 into Sleep mode. Sleep mode differs from Standby mode in that the PLL is powered down. To wake up from Sleep mode, use the RUN_SYS command.

Functions performed:
1. Wait for all modules to be idle (HMEM, I2C, SPI, PWR, 3-wire, SDRAM, and DSPE)
2. Power Pin (Enter Off State)
3. SDRAM (Enter Self-Refresh Mode)
4. SDRAM (Wait for Self-Refresh Mode Entered)
5. Power Pin (Wait for Off State Entered)
6. Power Save (Enable)
7. PLL Power Down (Enable Power Down)

Next Command Blocking: Yes

9.5.6 INIT_SYS_RUN (0x06 + 0 parameters)

This command initializes the S1D13521 according to the requirements of the customer.

Functions performed:
1. Configure PLL (PLLM = 3
2. PLL RUN
3. PLL (Wait Lock)
4. Disable Power Save Mode
5. SDRAM Init (according to customer setting)
6. DSPE Init (according to customer setting)
7. PWRPIN Init
8. Wait SDRAM Init done and PWRPIN POWER-ON
9. Power State (Write 0x1)

Next Command Blocking: Yes

9.5.7 INIT_SYS_STBY (0x07 + 0 parameters)

This command initializes the S1D13521 according to the requirements of the customer and places the S1D13521 into Standby mode.

Functions performed:
1. Configure PLL (PLLM = 3
2. PLL RUN
3. PLL (Wait Lock)
4. Disable Power Save Mode
5. SDRAM Init (according to customer setting)
6. DSPE Init (according to customer Setting)
7. PWRPIN Init
8. SDRAM Enter Self Refresh Mode, Power-Pin Off State
9. Power State (Write 0x2)
10. Enter Power Save Mode.

Next Command Blocking: Yes

9.5.8 INIT_SDRAM (0x08 + 4 parameters)

This command initializes the SDRAM.

Functions performed:
1. Setup the SDRAM registers using the specified parameters
2. Initialize the SDRAM
3. Wait for the SDRAM Initialize to complete

Next Command Blocking: Yes

Parameter 1

SDRAM Power Down Disable	SDRAM Refresh Cycle Time bits 1-0			SDRAM Refresh Rate bits 1-0		SDRAM Row Active Time bits 1-0	
15	14	13	12	11	10	9	8
16-bit SDRAM Enable	SDRAM tRP Latency Select	SDRAM tRCD Latency Select	SDRAM tCL Latency Select	n/a	SDRAM Column Address Count bits 1-0		SDRAM Burst Type Select
7	6	5	4	3	2	1	0

bit 15 SDRAM Power Down Disable
This bit controls the SDRAM power down function which dynamically disables the SDRAM clock when the SDRAM is idle.
When this bit = 0b, the SDRAM power down function is enabled.
When this bit = 1b, the SDRAM power down function is disabled.

bits 14-12 SDRAM Refresh Cycle Time bits [2:0]
These bits specify the SDRAM Refresh Cycle Time (tRFC) using the following formula.
Refresh cycle time = REG[0100h] bits 14-12 + 4

bits 11-10 SDRAM Refresh Rate bits [1:0]

These bits specify the SDRAM refresh rate for 8192 rows.

Table 9-6 : SDRAM Refresh Rate Selection

REG[0100h] bits 11-10	Refresh Rate
00b	64 ms
01b	128 ms
10b	256 ms
11b	512 ms

bits 9-8 SDRAM Row Active Time bits [1:0]

These bits specify the Row Active Time (tRAS) which defines the minimum time for an opened row to be issued a precharge.

Table 9-7 : SDRAM Row Active Time (tRAS) Selection

REG[0100h] bits 9-8	Row Active Time
00b	5 clocks
01b	6 clocks
10b	7 clocks
11b	8 clocks

bit 7 16-bit SDRAM Enable

This bit specifies whether 16 or 32-bit SDRAM is selected.

When this bit = 0b, 32-bit SDRAM mode is selected.

When this bit = 1b, 16-bit SDRAM mode is selected.

bit 6 SDRAM tRP Latency Select

This bit selects the Row Precharge Time which is the precharge time required before a row can be activated again.

When this bit = 0b, the row precharge time is 2 clocks.

When this bit = 1b, the row precharge time is 3 clocks.

bit 5 SDRAM tRCD Latency Select

This bit selects the Row to Column Latency.

When this bit = 0b, the row to column latency is 2 clocks.

When this bit = 1b, the row to column latency is 3 clocks.

bit 4 SDRAM tCL Latency Select

This bit selects the Column Read to Data Available Latency.

When this bit = 0b, the column read to data available latency is 2 clocks.

When this bit = 1b, the column read to data available latency is 3 clocks.

bits 2-1 SDRAM Column Address Count bits [1:0]

This bit specifies the number of column addresses used for the SDRAM.

Table 9-8 : SDRAM Column Address Count Selection

REG[0100h] bits 2-1	Column Address Count
00b	256
01b	512
10b	1024
11b	2048

bit 0 SDRAM Burst Type Select

This bit selects the type of burst used for SDRAM accesses.

When this bit = 0b, full page burst is selected. This setting is used for standard SDRAM.

When this bit = 1b, fixed 8-burst is selected. This setting is used for mobile SDRAM.

Parameter 2

SDRAM Refresh Clock Divide Select bits 15-8							
15	14	13	12	11	10	9	8
SDRAM Refresh Clock Divide Select bits 7-0							
7	6	5	4	3	2	0	0

bits 15-0 SDRAM Refresh Clock Divide Select bits [15:0]

These bits select the divide used to determine the SDRAM Refresh Clock frequency. These bits should be set such that the resulting refresh clock is approximately 64KHz. For further information on the clock structure, see Section Chapter 7, “Clocks” on page 45.

Refresh Clock Divide = REG[0106h] bits 15-0 + 1

The refresh clock is calculated using the following formula.

Refresh clock frequency = CLKI frequency ÷ Refresh Clock Divide

For example, the default register value of 02EDh results in the following refresh frequency when CLKI is 24MHz.

Refresh clock frequency = 24MHz ÷ 375
= 64KHz

Parameter 3

n/a							
15	14	13	12	11	10	9	8
n/a		0	0	1	n/a		
7	6	5	4	3	2	1	0

Parameter 3 must be set to 08h.

Parameter 4							
n/a	SDRAM Driver Strength bits 1-0		Temperature Compensated Self Refresh bits 1-0		Partial Array Self Refresh bits 2-0		
15	14	13	12	11	10	9	8
n/a					SDRAM Size bits 1-0		Extended Mode Register Program on Initialization Enable
7	6	5	4	3	2	1	0

bits 14-13 SDRAM Driver Strength bits [1:0]

These bits only have an effect when the Extended Mode Register Program On Initialization Enable bit is set to 1b, REG[010Ah] bit 0 = 1b. These bits set the value for Driver Strength (DS) that is programmed into the extended mode register of the mobile SDRAM.

Table 9-9 : SDRAM Driver Strength Selection

bits 14-13	Driver Strength
00b	Full Strength
01b	Half Strength
10b	Quarter Strength
11b	Eighth Strength

bits 12-11 Temperature Compensated Self Refresh bits [1:0]

These bits only have an effect when the Extended Mode Register Program On Initialization Enable bit is set to 1b, REG[010Ah] bit 0 = 1b. Mobile SDRAM allows the self refresh rate to be varied based on the temperature of the SDRAM. These bits set the value for Temperature Compensated Self Refresh (TCSR) that is programmed into the extended mode register of the mobile SDRAM.

bits 10-8 Partial Array Self Refresh bits [2:0]

These bits only have an effect when the Extended Mode Register Program On Initialization Enable bit is set to 1b, REG[010Ah] bit 0 = 1b. These bits set the value for Partial Array Self Refresh (PASR) that is programmed into the extended mode register of the mobile SDRAM.

bits 2-1 SDRAM Size bits [1:0]

These bits specify the SDRAM size, in M bytes. This setting is used for bank address placement.

Table 9-10 : SDRAM Size Selection

bits 2-1	SDRAM Size
00b	8M bytes
01b	16M bytes
10b	32M bytes
11b	64M bytes

bit 0 Extended Mode Register Program On Initialization Enable
When mobile SDRAM is used, this bit controls whether the extended mode register is programmed when the SDRAM is initialized, REG[0102h] bit 0 = 1b.
When this bit = 0b, the extended mode register is not programmed when the SDRAM is initialized.
When this bit = 1b, the extended mode register is programmed when the SDRAM is initialized.

9.5.9 INIT_DSPE_CFG (0x09 + 5 parameters)

This command initializes the Display Engine.

Functions performed:
1. Initializes the Display Engine according to the specified parameters
2. Set REG[032Ch] to 0x0400, Area Size Mode Enabled

Parameter 1

15	14	13	12	11	10	9	8
Panel HSize bits 15-8							
7	6	5	4	3	2	1	0
Panel HSize bits 7-0							

Parameter 2

15	14	13	12	11	10	9	8
Panel VSize bits 15-8							
7	6	5	4	3	2	1	0
Panel VSize bits 7-0							

Parameter 3

15	14	13	12	11	10	9	8
Source Driver Chip Enable Start bits 3-0				Source Driver Pixel Output Count Select	Source Driver Chip Enable Reverse	Source Driver Output Reverse	Source Driver Shift Right
7	6	5	4	3	2	1	0
Source Driver Output Size Select bits 7-0							

Parameter 4

15	14	13	12	11	10	9	8
n/a						Source Driver Swap Padding Pixels	Source Driver Early SDOE Assert Disable
7	6	5	4	3	2	1	0
n/a						Gate Driver Right/Left Select	Gate Driver Start Pulse Polarity

Parameter 5

15	14	13	12	11	10	9	8
Display Engine Software Reset (WO)	n/a						
7	6	5	4	3	2	1	0
LUT Auto Select Enable	n/a				LUT Index Format Select bits 2-0		

9.5.10 INIT_DSPE_TMG (0x0A + 5 parameters)

This command initializes the display timing information.

Functions performed:
1. Initialize the Display Engine display timing according to parameters 1-4
2. Initialize the Pixel Clock according to parameter 5

Parameter 1							
n/a							
15	14	13	12	11	10	9	8
Frame Sync Length bits 7-0							
7	6	5	4	3	2	1	0

Parameter 2							
Frame End Length bits 7-0							
15	14	13	12	11	10	9	8
Frame Begin Length bits 7-0							
7	6	5	4	3	2	1	0

Parameter 3							
n/a							
15	14	13	12	11	10	9	8
Line Sync Length bits 7-0							
7	6	5	4	3	2	1	0

Parameter 4							
Line End Length bits 7-0							
15	14	13	12	11	10	9	8
Line Begin Length bits 7-0							
7	6	5	4	3	2	1	0

Parameter 5							
n/a							
15	14	13	12	11	10	9	8
n/a			Pixel Clock Bypass Enable	Pixel Clock Divide Select bits 3-0			
7	6	5	4	3	2	1	0

9.5.11 INIT_ROTMODE (0x0B + 1 parameter)

This command initializes the S1D13521 Rotation Mode

Functions performed:
1. Set REG[032Ch] bits 9-8 with the specified Rotation Mode
2. Set REG[0140h] bits 9-8 with the specified Rotation Mode

Parameter 1							
n/a						Rotation Mode bits 1-0	
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0

9.5.12 RD_REG (0x10 + 2 parameters)

This command initiates a low level register read from the address specified by parameter 1. The returned data value is available in parameter 2.

Parameter 1							
Register Address bits 15-8							
15	14	13	12	11	10	9	8
Register Address bits 7-0							
7	6	5	4	3	2	1	0

Parameter 2							
Register Read Data bits 15-8							
15	14	13	12	11	10	9	8
Register Read Data bits 7-0							
7	6	5	4	3	2	1	0

9.5.13 WR_REG (0x11 + 2 parameters)

This command initiates a low level register write of the data specified by parameter 2 to the address specified by parameter 1..

Parameter 1							
Register Address bits 15-8							
15	14	13	12	11	10	9	8
Register Address bits 7-0							
7	6	5	4	3	2	1	0

Parameter 2							
Register Write Data bits 15-8							
15	14	13	12	11	10	9	8
Register Write Data bits 7-0							
7	6	5	4	3	2	1	0

9.5.14 RD_SFM (0x12 + 0 parameters)

This command initiates a low level read from the Serial Flash Memory.

9.5.15 WR_SFM (0x13 + 1 parameter)

This command initiates low level write of the data specified by parameter 1 to the Serial Flash Memory.

Parameter 1							
15	14	13	12	11	10	9	8
Serial Flash Memory Write Data bits 7-0							
7	6	5	4	3	2	1	0

9.5.16 END_SFM (0x14 + 0 parameters)

This command ends a low level operation to/from the Serial Flash Memory.

9.5.17 BST_RD_SDR (0x1C + 4 parameters)

This command starts a memory burst read operation.

Functions performed:
1. End Previous Host Memory access operation if currently active.
2. Setup Read Mode and Raw Access Mode on REG[0140h]
3. Setup Raw Address
4. Setup Burst Size
5. Trigger Start and Wait for Ready..

Parameter 1							
Memory Address bits 15-8							
15	14	13	12	11	10	9	8
Memory Address bits 7-0							
7	6	5	4	3	2	1	0

Parameter 2							
Memory Address bits 31-24							
15	14	13	12	11	10	9	8
Memory Address bits 23-16							
7	6	5	4	3	2	1	0

Parameter 3							
Burst Size bits 15-8							
15	14	13	12	11	10	9	8
Burst Size bits 7-0							
7	6	5	4	3	2	1	0

Parameter 4							
Burst Size bits 31-24							
15	14	13	12	11	10	9	8
Burst Size bits 23-16							
7	6	5	4	3	2	1	0

9.5.18 BST_WR_SDR (0x1D + 4 parameters)

This command starts a memory burst write operation.

Functions performed:
1. End Previous Host Memory access operation if currently active.
2. Setup Write Mode and Raw Access Mode on REG[0140h]
3. Setup Raw Address
4. Setup Burst Size
5. Trigger Start and Wait for Ready....

Parameter 1							
Memory Address bits 15-8							
15	14	13	12	11	10	9	8
Memory Address bits 7-0							
7	6	5	4	3	2	1	0

Parameter 2							
Memory Address bits 31-24							
15	14	13	12	11	10	9	8
Memory Address bits 23-16							
7	6	5	4	3	2	1	0

Parameter 3							
Burst Size bits 15-8							
15	14	13	12	11	10	9	8
Burst Size bits 7-0							
7	6	5	4	3	2	1	0

Parameter 4							
Burst Size bits 31-24							
15	14	13	12	11	10	9	8
Burst Size bits 23-16							
7	6	5	4	3	2	1	0

9.5.19 BST_END_SDR (0x1E + 0 parameters)

This command terminates a burst operation before it has completed.

Functions performed:
1. End Previous Host Memory access operation if currently active
2. Wait for Busy to end

9.5.20 LD_IMG (0x20 + 1 parameter)

This command starts a Full Frame Memory Load operation according to the data packing settings in parameter 1.

Functions performed:
1. End Previous Host Memory access operation if currently active.
2. Setup Write Mode and Packed Access Mode on REG[0140h]
3. Setup Packing Bpp Select using Parameter
4. Setup Full Display Size Update (Copy size from Display Engine's registers)
5. Trigger start transfer.

Parameter 1							
n/a							
15	14	13	12	11	10	9	8
n/a		Data Packing Select bits 1-0		n/a			
7	6	5	4	3	2	1	0

9.5.21 LD_IMG_AREA (0x22 + 5 parameters)

This command starts an Area Defined Frame Memory Load operation according to the data packing settings in the parameters.

Functions performed:
1. End Previous Host Memory access operation if currently active.
2. Setup Write Mode and Packed Access Mode on REG[0140h]
3. Setup Packing Bpp Select using Parameter
4. Setup Size with Parameters.
5. Trigger start transfer

Parameter 1

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a		Data Packing Select bits 1-0		n/a			

Parameter 2

15	14	13	12	11	10	9	8
n/a			Packed Pixel Rectangular X-Start Position bits 12-8				
7	6	5	4	3	2	0	0
Packed Pixel Rectangular X-Start Position bits 7-0							

Parameter 3

15	14	13	12	11	10	9	8
n/a			Packed Pixel Rectangular Y-Start Position bits 12-8				
7	6	5	4	3	2	0	0
Packed Pixel Rectangular Y-Start Position bits 7-0							

Parameter 4

15	14	13	12	11	10	9	8
n/a			Packed Pixel Rectangular Width bits 12-8				
7	6	5	4	3	2	0	0
Packed Pixel Rectangular Width bits 7-0							

Parameter 5

15	14	13	12	11	10	9	8
n/a			Packed Pixel Rectangular Height bits 12-8				
7	6	5	4	3	2	0	0
Packed Pixel Rectangular Height bits 7-0							

9.5.22 LD_IMG_END (0x23 + 0 parameters)

This command terminates a Load Image operation before it has completed and waits for the image load to finish before writing to the Memory.

Functions performed:
1. End Previous Host Memory access operation if currently active.
2. Wait for Busy to end

9.5.23 LD_IMG_WAIT (0x24 + 0 parameters)

This command waits for a Load Image operation to finish writing to the memory.

Functions performed:
1. Wait for REG[0140h] bit 12 - wait for busy to deassert.

9.5.24 LD_IMG_SETADR (0x25 + 2 parameters)

This command loads an image to the address specified by the Host (see REG[0144h] ~ REG[0146h]).

9.5.25 LD_IMG_DSPEADR (0x26 + 0 parameters)

This command loads an image to the address specified by the Display Engine image buffer (see REG[0310h] ~ REG[0312h]).

9.5.26 WAIT_DSPE_TRG (0x28 + 0 parameters)

This command waits for the Display Engine operation to complete.

Functions performed:
1. Wait for REG[0338h] bit 0 to return 0b

9.5.27 WAIT_DSPE_FREND (0x29 + 0 parameters)

This command wait for the Display Engine to complete outputting display frames.

Functions performed:
1. Wait for REG[0338h] bit 3 to return 0b

9.5.28 WAIT_DSPE_LUTFREE (0x2A + 0 parameters)

This command wait for the Display Engine to have at least one free LUT.

Functions performed:
1. Wait for REG[0338h] bit 6 to return 1b

9.5.29 WAIT_DSPE_MLUTFREE (0x2B + 1 parameter)

This command waits for the Display Engine to have at least one free Masked LUT.

Functions performed:
1. Setup LUT Mask register with parameter 1
2. Wait for REG[0338h] bit 7 to return 1b

Parameter 1							
LUT Mask Setting 15:8							
15	14	13	12	11	10	9	8
LUT Mask Setting 7:0							
7	6	5	4	3	2	1	0

9.5.30 RD_WFM_INFO (0x30 + 2 parameters)

This command issues a Waveform Read operation to the Display Engine.

Functions performed:
1. Setup Waveform Address
2. Trigger Waveform Read operation
3. Wait for Trigger completed

Parameter 1							
Waveform Header Serial Flash Address bits 15-8							
15	14	13	12	11	10	9	8
Waveform Header Serial Flash Address bits 7-0							
7	6	5	4	3	2	1	0

Parameter 2							
n/a							
15	14	13	12	11	10	9	8
Waveform Header Serial Flash Address bits 23-16							
7	6	5	4	3	2	1	0

9.5.31 UPD_INIT (0x32 + 0 parameters)

This command issues an Update Buffer Refresh with data from the Image Buffer. No display operation will occur.

9.5.32 UPD_FULL (0x33 + 1 parameter)

This command issues a Full Frame Full Update operation to the Display Engine.

Parameter 1							
n/a	Border Update Enable	n/a		Display Update Waveform Mode bits 3-0			
15	14	13	12	11	10	9	8
Display Update LUT Select bits 3-0				n/a			
7	6	5	4	3	2	1	0

9.5.33 UPD_FULL_AREA (0x34 + 5 parameters)

This command issues an Area Defined Full Update operation to the Display Engine.

Functions performed:
1. Setup Display Engine Area Search Dimension
2. Trigger Full Area update with Parameter 1.

Parameter 1

15	14	13	12	11	10	9	8
n/a	Border Update Enable	n/a		Display Update Waveform Mode bits 3-0			
7	6	5	4	3	2	1	0
Display Update LUT Select bits 3-0				n/a			

Parameter 2

15	14	13	12	11	10	9	8
Area Update Pixel Rectangular X-Start Position bits 11-8							
7	6	5	4	3	2	0	0
Area Update Pixel Rectangular X-Start Position bits 7-0							

Parameter 3

15	14	13	12	11	10	9	8
Area Update Pixel Rectangular Y-Start Position bits 15-8							
7	6	5	4	3	2	0	0
Area Update Pixel Rectangular Y-Start Position bits 7-0							

Parameter 4

15	14	13	12	11	10	9	8
Area Update Pixel Rectangular Width bits 15-8							
7	6	5	4	3	2	0	0
Area Update Pixel Rectangular Width bits 7-0							

Parameter 5

15	14	13	12	11	10	9	8
Area Update Pixel Rectangular Height bits 15-8							
7	6	5	4	3	2	0	0
Area Update Pixel Rectangular Height bits 7-0							

9.5.34 UPD_PART (0x35 + 1 parameter)

This command issues a Partial Update operation to the Display Engine. This operation affects changed pixels only.

Functions performed:
1. Trigger Partial update with Parameter 1

Parameter 1

15	14	13	12	11	10	9	8
n/a	Border Update Enable	n/a		Display Update Waveform Mode bits 3-0			
7	6	5	4	3	2	1	0
Display Update LUT Select bits 3-0				n/a			

9.5.35 UPD_PART_AREA (0x36 + 5 parameters)

This command issues an Area defined Partial Update operation to the Display Engine. This operation affects changed pixels only.

Functions performed:
1. Setup Display Engine Area Search Dimension
2. Trigger Full Area update with Parameter 1.

Parameter 1							
n/a	Border Update Enable	n/a		Display Update Waveform Mode bits 3-0			
15	14	13	12	11	10	9	8
Display Update LUT Select bits 3-0				n/a			
7	6	5	4	3	2	1	0

Parameter 2							
Area Update Pixel Rectangular X-Start Position bits 11-8							
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular X-Start Position bits 7-0							
7	6	5	4	3	2	0	0

Parameter 3							
Area Update Pixel Rectangular Y-Start Position bits 15-8							
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular Y-Start Position bits 7-0							
7	6	5	4	3	2	0	0

Parameter 4							
Area Update Pixel Rectangular X-End Position bits 15-8							
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular X-End Position bits 7-0							
7	6	5	4	3	2	0	0

Parameter 5							
Area Update Pixel Rectangular Y-End Position bits 15-8							
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular Y-End Position bits 7-0							
7	6	5	4	3	2	0	0

9.5.36 UPD_GDRV_CLR (0x37 + 0 parameters)

This command issues a display sequence output on the Gate Driver only. This command is used to clear the unknown state of the Gate Driver display at power-up.

9.5.37 UPD_SET_IMGADR (0x38 + 2 parameters)

This command sets the Display Engine Image Buffer Start Address.

Parameter 1							
Image Buffer Start Address bits 15-8							
15	14	13	12	11	10	9	8
Image Buffer Start Address bits 7-0							
7	6	5	4	3	2	1	0

Parameter 2							
Image Buffer Start Address bits 31-24							
15	14	13	12	11	10	9	8
Image Buffer Start Address bits 23-16							
7	6	5	4	3	2	1	0

Chapter 10 Registers

This section discusses how and where to access the S1D13521 registers. It also provides detailed information about the layout and usage of each register.

10.1 Register Access

The S1D13521 registers are 16-bit wide. They can be accessed using the Command Interface

10.1.1 Register Access using Command Interface

Registers may be accessed using the command interface with the following sequences.

For single 16-bit register reads:

Table 10-1: Register Read Sequence

Tx Count	16-bit Indirect Host
0	Write Code[15:0] <= 0x0010
1	Write Register Address[15:0]
2	Read

For single 16-bit register writes:

Table 10-2: Register Write Sequence

Tx Count	16-bit Indirect Host
0	Write Code[15:0] <= 0x0011
1	Write Register Address[15:0]
2	Write

Note
Only single register accesses are supported (i.e. register address is not auto incremented to the next register address).

Table 10-3: Register Mapping

Address Range	Register Type	Description
0000h to 000Fh	Asynchronous	System Configuration Registers
0010h to 001Fh	Asynchronous	Clock Configuration Registers
0020h to 002Fh	Asynchronous	Component Configuration
0100h to 010Fh	Synchronous	Memory Controller Configuration
0140h to 015Fh	Synchronous	Host Interface Memory Access Configuration
0200h to 020Fh	Synchronous	SPI Flash Memory Interface
0210h to 011Fh	Synchronous	I2C Thermal Sensor Interface Registers
0220h to 022Fh	Synchronous	3-Wire Chip Interface Registers
0230h to 023Fh	Synchronous	Power Pin Control Configuration Registers
0240h to 024Fh	Synchronous	Interrupt Configuration Registers
0250h to 025Fh	Synchronous	GPIO Control Registers
0300h to 03FFh	Synchronous	Display Engine Registers

10.2 Register Set

The S1D13521 registers are listed in the following table.

Table 10-4: S1D13521 Register Set

Table 10-4: S1D13521 Register Set (Continued)

Register	Pg	Register	Pg
REG[0294h] Command RAM Controller Access Port Register	119		
Command Sequencer Controller Registers			
REG[02A0h] Command Sequencer Controller Index Register	120	REG[02A2h] Command Sequencer Controller Data Port Register	120
Display Engine: Display Timing Configuration			
REG[0300h] Frame Data Length Register	121	REG[0302h] Frame Sync Length Register	121
REG[0304h] Frame Begin/End Length Register	121	REG[0306h] Line Data Length Register	122
REG[0308h] Line Sync Length Register	122	REG[030Ah] Line Begin/End Length Register	122
Display Engine: Driver Configurations			
REG[030Ch] Source Driver Configuration Register	123	REG[030Eh] Gate Driver Configuration Register	125
Display Engine: Memory Region Configuration Registers			
REG[0310h] Image Buffer Start Address Register 0	126	REG[0312h] Image Buffer Start Address Register 1	126
REG[0314h] Update Buffer Start Address Register 0	126	REG[0316h] Update Buffer Start Address Register 1	126
Display Engine: Component Control			
REG[0320h] Temperature Device Select Register	127	REG[0322h] Temperature Value Register	127
REG[0324h] DWELL Time Configuration Register	127	REG[0326h] Border Configuration Register 0	128
REG[0328h] Border Configuration Register 1	128	REG[032Ah] Power Control Configuration Register	129
REG[032Ch] General Configuration Register	130	REG[032Eh] LUT Mask Register	131
Display Engine: Control/Trigger Registers			
REG[0330h] Update Buffer Configuration Register	132	REG[0332h] Update Buffer Pixel Set Value Register	133
REG[0334h] Display Engine Control/Trigger Register	133		
Display Engine: Update Buffer Status Registers			
REG[0336h] Lookup Table Status Register	135	REG[0338h] Display Engine Busy Status Register	135
Display Engine: Interrupt Registers			
REG[033Ah] Display Engine Interrupt Raw Status Register	138	REG[033Ch] Display Engine Interrupt Masked Status Register	141
REG[033Eh] Display Engine Interrupt Enable Register	144		
Display Engine: Partial Update Configuration Register			
REG[0340h] Area Update Pixel Rectangular X-Start Register	147	REG[0342h] Area Update Pixel Rectangular Y-Start Register	147
REG[0344h] Area Update Pixel Rectangular X-End / Horizontal Size Register	147	REG[0346h] Area Update Pixel Rectangular Y-End / Vertical Size Register	147
REG[0348h] Host Pixel Rectangular X-Start Register	148	REG[034Ah] Host Pixel Rectangular Y-Start Register	148
REG[034Ch] Host Pixel Rectangular X-End Register	148	REG[034Eh] Host Pixel Rectangular Y-End Register	148
Display Engine: Serial Flash Waveform Registers			
REG[0350h] Waveform Header Serial Flash Address Register 0	149	REG[0352h] Waveform Header Serial Flash Address Register 0	149
REG[0354h] through REG[035Eh] are Reserved			

10.3 Register Descriptions

10.3.1 System Configuration Registers

REG[0000h] Revision Code Register
Default = 0000h — Read Only

15	14	13	12	11	10	9	8
Revision Code bits 15-8							
7	6	5	4	3	2	1	0
These bits always return 0000_0000b							

bits 7-0 These bits always return 0000_0000b.

bits 15-8 Revision Code bits [7:0] (Read Only)
These bits indicate the revision code.
The revision code for the S1D13521 is 00h.

REG[0002h] Product Code Register
Default = 0047h — Read Only

15	14	13	12	11	10	9	8
Product Code bits 15-8							
7	6	5	4	3	2	1	0
Product Code bits 7-0							

bits 15-0 Product Code bits [15:0] (Read Only)
These bits indicate the product code.
The product code for the S1D13521 is 0047h.

REG[0004h] Config Pin Read Value Register
Default = 000Xh — Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a					CNF[2:0] Status		

bits 2-0 CNF[2:0] Status (Read Only)
These bits return the status of the configuration pins CNF[2:0]. For a functional description of each CNF[2:0] pin, see Section 4.2.10, “Miscellaneous” on page 20.

REG[0006h] Power Save Mode Register
Default = 0001h — Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a							Power Save Mode Enable

bit 0 Power Save Mode Enable

This bit controls power save mode.
When this bit = 0b, power save mode is disabled.
When this bit = 1b, power save mode is enabled and all clocks are gated off. (default)

This bit in combination with the PLL Power Down (REG[0016h] bit 1) and PLL Bypass (REG[0016h] bit 0) bits, define the different power states of the S1D13521. The following table summarizes the possible states of the S1D13521.

Table 10-5: S1D13521 Power States Summary

Power State	Power Save Mode Enable (REG[0006h] bit 0)	PLL Power Down (REG[0016h] bit 1)	PLL Bypass (REG[0016h] bit 0)
OFF	1b	1b	1b
SLEEP	1b	1b	1b
STANDBY (PLL) (See Note)	1b	0b	0b
RUN (PLL)	0b	0b	0b
RUN (CLKI)	0b	1b	1b

Note
When STANDBY (PLL) is selected, all internal clocks are gated off but the PLL remains running. This is done to avoid waiting for the PLL to become stable (PLL lock time) before returning to the RUN (PLL) state. There is no STANDBY (CLKI) state.

REG[0008h] Software Reset Register
Default = 0000h — Write Only

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a							Software Reset

bit 0 Software Reset (Write Only)

This bit performs a software reset of the S1D13521 which sets all registers to their default states and all pins to their RESET# states.
Writing a 0b to this bit has no hardware effect.
Writing a 1b to this bit initiates a software reset of the S1D13521.

REG[000Ah] System Status Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
3-Wire Busy Status (RO)	Power Management Busy Status (RO)	n/a	Power Save Status bits 2-0			SDRAM Self Refresh Mode Status (RO)	Power Management Power Sequence Status (RO)
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C Busy Status (RO)	SPI Busy Status (RO)	Host Interface Busy Status (RO)	SDRAM Controller Busy Status (RO)	Host Memory Access Busy Status (RO)	Display Engine Busy Status (RO)	SDRAM Initialized (RO)	PLL Lock (RO)

bit 15 3-Wire Busy Status (Read Only)
This bit indicates the status for 3-Wire.
When this bit = 0b, 3-Wire is not busy.
When this bit = 1b, 3-Wire is busy.

bit 14 Power Management Busy Status (Read Only)
This bit indicates the status of the Power Management logic.
When this bit = 0b, the Power Management logic is not busy.
When this bit = 1b, the Power Management logic is busy.

bits 12-10 Power Save Status bits [2:0]
These bits indicate the power save status of the S1D13521.

Table 10-6 : Power Save Status

REG[000Ah] bits 12-10	Power Save Status
000b	Unknown
001b	Normal Operation
010b	Standby Mode
011b	Sleep Mode
100b ~ 111b	Reserved

bit 9 SDRAM Self Refresh Mode Status (Read Only)
This bit indicates whether the SDRAM controller is in self refresh mode. SDRAM self refresh mode is controlled using the SDRAM Enter Self Refresh Trigger bit (REG[0104h] bit 0) and the SDRAM Exit Self Refresh Trigger bit (REG[0104h] bit 1).
When this bit = 0b, the SDRAM controller is not in self refresh mode.
When this bit = 1b, the SDRAM controller is in self refresh mode.

bit 8 Power Management Power Sequence Status (Read Only)
This bit provides the status of the power management sequence. For further information, see Section 6.6, “Power Pin Interface” on page 43.
When this bit = 0b, it is currently in a power off state. (default)
When this bit = 1b, it is currently in a power on state.

bit 7 I2C Busy Status (Read Only)
This bit indicates whether the I2C interface is busy.
When this bit = 0b, the I2C interface is idle (not busy).
When this bit = 1b, the I2C interface is busy.

bit 6 SPI Busy Status (Read Only)
This bit indicates whether the SPI interface is busy.
When this bit = 0b, the SPI interface is idle (not busy).
When this bit = 1b, the SPI interface is busy.

bit 5 Host Command Interface Busy Status (Read Only)
This bit indicates whether the Host Command interface is busy.
When this bit = 0b, the Host Command interface is idle (not busy).
When this bit = 1b, the Host Command interface is busy.

bit 4 SDRAM Controller Busy Status (Read Only)
This bit indicates whether the SDRAM controller is busy.
When this bit = 0b, the SDRAM controller is idle (not busy).
When this bit = 1b, the SDRAM controller is busy.

bit 3 Host Memory Access Busy Status (Read Only)
This bit indicates whether a Host Memory Access is taking place.
When this bit = 0b, a Host Memory Access is not taking place (not busy).
When this bit = 1b, a Host Memory Access is taking place (busy).

bit 2 Display Engine Busy Status (Read Only)
This bit indicates whether the Display Engine is busy.
When this bit = 0b, the Display Engine is idle (not busy).
When this bit = 1b, the Display Engine is busy.

bit 1 SDRAM Initialized (Read Only)
This bit indicates whether the SDRAM has been initialized. The SDRAM initialization sequence is triggered by the SDRAM Initialization Trigger bit, REG[0102h] bit 0.
When this bit = 0b, the SDRAM has not been initialized.
When this bit = 1b, the SDRAM has been initialized.

bit 0 PLL Lock (Read Only)
This bit indicates whether the PLL output is stable (locked). The S1D13521 synchronous registers (see Table 10-3: “Register Mapping,” on page 76) and the external SDRAM must not be accessed before the PLL output is stable.
When this bit = 0b, the PLL output is not stable.
When this bit = 1b, the PLL output is stable.

10.3.2 Clock Configuration Registers

REG[0010h] PLL Configuration Register 0
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
PLL Setting 0 bits 7-0							
7	6	5	4	3	2	1	0
n/a		M-Divider bits 5-0					

bits 15-8 PLL Setting 0 bits [7:0]
These bits must be set to F8h.

bits 5-0 M-Divider bits [5:0]
These bits determine the divide ratio between CLKI and the actual input clock to the PLL. These bits must be set such that the internal input clock to the PLL (PLLCLK) is between 20MHz and 66.5MHz.

Table 10-7: PLL M-Divide Selection

REG[10h] bits 5-0	M-Divider Ratio
0h	1:1
01h	2:1
02h	3:1
03h	4:1
• • •	• • •
20h	33:1
21h to 3Fh	Reserved

REG[0012h] PLL Configuration Register 1
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
PLL Setting 1 bits 15-8							
7	6	5	4	3	2	1	0
PLL Setting 1 bits 7-0							

bits 15-0 PLL Setting 1 bits [15:0]
These bits must be set to 2880h.

REG[0014h] PLL Configuration Register 2
Default = 0000h — Read/Write

n/a	L-Counter bits 6-0						
15	14	13	12	11	10	9	8
PLL Setting 2 bits 7-0							
7	6	5	4	3	2	1	0

bits 14-8 L-Counter bits [6:0]

These bits are used to configure the PLL Output (in MHz) and must be set according to the following formula.

PLL Output = (L-Counter + 1) x PLLCLK
= LL x PLLCLK

Where:
PLL Output is the desired PLL output frequency (in MHz).
L-Counter is the value of this register (in decimal).
PLLCLK is the internal input clock to the PLL (in MHz).

Table 10-8 PLL Setting Example

Target Frequency (MHz)	LL	CLKI Input Clock (MHz)	M-Divider REG[0010h] bits 5-0	M-Divide Ratio	PLLCLK (MHz)	POUT (MHz)
133	4	33	00h	1:1	33	132

bits 7-0 PLL Setting 2 bits [7:0]

These bits must be set to 00h.

REG[0016h] Clock Configuration Register
Default = 0002h — Read/Write

n/a							System Clock Divide Select
15	14	13	12	11	10	9	8
n/a						PLL Power Down Enable	PLL Bypass Mode Enable
7	6	5	4	3	2	1	0

bit 8 System Clock Divide Select

This bit selects the divide ratio used to generate the system clock which is derived from either the PLL output or the CLKI input depending on the PLL Bypass Select bit, REG[0016h] bit 0. The maximum frequency for the system clock is 66.5Mhz. For further details on the clock structure, see Section Chapter 7, “Clocks” on page 45.
When this bit = 0b, the divide ratio is 1:2.
When this bit = 1b, the divide ratio is 1:3.

bit 1 PLL Power Down Enable

This bit controls the PLL. Once the PLL is placed in a powered down state, enabling it will require a minimum of 1 ms before the PLL output is stable. The status of the PLL can be checked using the PLL Lock bit, REG[000Ah] bit 0. For further details on the clock structure, see Section Chapter 7, “Clocks” on page 45.

When this bit = 0b, the PLL is in active mode and PLL output is stable once REG[000Ah] bit 0 = 1b.

When this bit = 1b, the PLL is in power down mode. (default)

bit 0 PLL Bypass Mode Enable

This bit controls PLL Bypass Mode which determines whether the PLL output or the CLKI input is used as the internal clock. For further details on the clock structure, see Section Chapter 7, “Clocks” on page 45.

When this bit = 0b, PLL Bypass Mode is disabled (PLL output is used).

When this bit = 1b, PLL Bypass Mode is enabled (CLKI is used).

REG[0018h] Pixel Clock Configuration Register

Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a			Pixel Clock Divide Disable	Pixel Clock Divide Select bits 3-0			
7	6	5	4	3	2	1	0

bit 4 Pixel Clock Divide Disable

This bit controls whether the pixel clock source is divided or not.

When this bit = 0b, the Pixel Clock Divide Select bits (REG[0018h] bit 3-0) are used to determine the pixel clock.

When this bit = 1b, the pixel clock source is not divided (1:1). Note that this setting is not recommended for normal operations.

bits 3-0 Pixel Clock Divide Select bits [3:0]

These bits select the divide ratio for the Pixel Clock which is derived from either the PLL output or CLKI depending on the PLL Bypass Mode Enable bit, REG[0016h] bit 0. For further details on the clock structure, see Section Chapter 7, “Clocks” on page 45.

Table 10-9: Pixel Clock Divide Ratio Selection

REG[0018h] bits 3-0	Pixel Clock Divide Ratio
0000b	1:1.5
0001b	1:2
0010b	1:3
0011b	1:4
0100b	1:5
0101b	1:6
0110b	1:7
0111b	1:8

REG[0018h] bits 3-0	Pixel Clock Divide Ratio
1000b	1:9
1001b	1:10
1010b	1:11
1011b	1:12
1100b	1:13
1101b	1:14
1110b	1:16
1111b	1:64

REG[001Ah] I2C Thermal Sensor Clock Configuration Register

Default = 0007h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a				I2C Thermal Sensor Clock Divide Select bits 3-0			

bits 3-0 I2C Thermal Sensor Clock Divide Select bits [3:0]

These bits select the divide ratio for the I2C Thermal Sensor Clock which is derived from either the PLL output or CLKI depending on the PLL Bypass Mode Enable bit, REG[0016h] bit 0. For further details on the clock structure, see Section Chapter 7, “Clocks” on page 45.

The divide ratio is calculated using the following formula.

I2C Thermal Sensor Clock Divide Ratio = 1 : (REG[001Ah] bits 3-0 + 1)

Note

This clock must be set such that it satisfies the following equation:

Clock Divide = System Clock (50Mhz) / (16 x 400Khz)

10.3.3 Component Configuration

REG[0020h] Peripheral Device Configuration Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a							Power Line Management Select

bit 0 Power Line Management Select

This bit selects whether internally generated timing is used for power pin management or whether a Dialog DA8590 IC or compatible device is used power management. This bit must be set to 0b when a Dialog DA8590 IC or compatible device is not present.

When this bit = 0b, internal timing is used for power pin management.

When this bit = 1b, a Dialog DA8590 IC or compatible device is used for power management.

10.3.4 Memory Controller Configuration

REG[0100h] SDRAM Configuration Register
Default = 5070h — Read/Write

SDRAM Power Down Disable	SDRAM Refresh Cycle Time bits 1-0			SDRAM Refresh Rate bits 1-0		SDRAM Row Active Time bits 1-0	
15	14	13	12	11	10	9	8
16-bit SDRAM Enable	SDRAM tRP Latency Select	SDRAM tRCD Latency Select	SDRAM tCL Latency Select	n/a	SDRAM Column Address Count bits 1-0		SDRAM Burst Type Select
7	6	5	4	3	2	1	0

bit 15 SDRAM Power Down Disable

This bit controls the SDRAM power down function which dynamically disables the SDRAM clock when the SDRAM is idle.
When this bit = 0b, the SDRAM power down function is enabled.
When this bit = 1b, the SDRAM power down function is disabled.

bits 14-12 SDRAM Refresh Cycle Time bits [2:0]

These bits specify the SDRAM Refresh Cycle Time (tRFC) using the following formula.

Refresh cycle time = REG[0100h] bits 14-12 + 4

bits 11-10 SDRAM Refresh Rate bits [1:0]

These bits specify the SDRAM refresh rate for 8192 rows.

Table 10-10 : SDRAM Refresh Rate Selection

REG[0100h] bits 11-10	Refresh Rate
00b	64 ms
01b	128 ms
10b	256 ms
11b	512 ms

bits 9-8 SDRAM Row Active Time bits [1:0]

These bits specify the Row Active Time (tRAS) which defines the minimum time for an opened row to be issued a precharge.

Table 10-11 : SDRAM Row Active Time (tRAS) Selection

REG[0100h] bits 9-8	Row Active Time
00b	5 clocks
01b	6 clocks
10b	7 clocks
11b	8 clocks

bit 7 16-bit SDRAM Enable

This bit specifies whether 16 or 32-bit SDRAM is selected.
When this bit = 0b, 32-bit SDRAM mode is selected.
When this bit = 1b, 16-bit SDRAM mode is selected.

bit 6 SDRAM tRP Latency Select
This bit selects the Row Precharge Time which is the precharge time required before a row can be activated again.
When this bit = 0b, the row precharge time is 2 clocks.
When this bit = 1b, the row precharge time is 3 clocks.

bit 5 SDRAM tRCD Latency Select
This bit selects the Row to Column Latency.
When this bit = 0b, the row to column latency is 2 clocks.
When this bit = 1b, the row to column latency is 3 clocks.

bit 4 SDRAM tCL Latency Select
This bit selects the Column Read to Data Available Latency.
When this bit = 0b, the column read to data available latency is 2 clocks.
When this bit = 1b, the column read to data available latency is 3 clocks.

bits 2-1 SDRAM Column Address Count bits [1:0]
This bit specifies the number of column addresses used for the SDRAM.

Table 10-12 : SDRAM Column Address Count Selection

REG[0100h] bits 2-1	Column Address Count
00b	256
01b	512
10b	1024
11b	2048

bit 0 SDRAM Burst Type Select
This bit selects the type of burst used for SDRAM accesses.
When this bit = 0b, full page burst is selected. This setting is used for standard SDRAM.
When this bit = 1b, fixed 8-burst is selected. This setting is used for mobile SDRAM.

REG[0102h] SDRAM Init Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							SDRAM Initialization Complete (RO)

7	6	5	4	3	2	1	0
n/a						SDRAM Initialization Wait Select	SDRAM Initialization Trigger (WO)

bit 8 SDRAM Initialization Complete (Read Only)
This bit indicates the initialization status of the SDRAM. Once SDRAM has been initialized, this bit will remain high until the S1D13521 is reset.
When this bit = 0b, the SDRAM has not been initialized.
When this bit = 1b, the SDRAM has been initialized.

bit 1 SDRAM Initialization Wait Select
This bit selects the minimum amount of wait time required by the SDRAM before starting the initialization sequence.
When this bit = 0b, the minimum wait time is 100µs (i.e. Micron SDRAM).
When this bit = 1b, the minimum wait time is 200µs (i.e. Samsung SDRAM).

bit 0 SDRAM Initialization Trigger (Write Only)
This bit triggers the SDRAM initialization sequence. The initialization status of the SDRAM is indicated by the SDRAM Initialization Complete bit, REG[0102h] bit 8.
Writing a 0b to this bit has no effect.
Writing a 1b to this bit initiates the SDRAM initialization sequence.

REG[0104h] SDRAM State Trigger Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							SDRAM Self Refresh Mode State (RO)
7	6	5	4	3	2	1	0
n/a						SDRAM Exit Self Refresh Trigger (WO)	SDRAM Enter Self Refresh Trigger (WO)

bit 8 SDRAM Self Refresh Mode State (Read Only)
This bit indicates whether the SDRAM is in Self Refresh mode or not.
When this bit = 0b, the SDRAM is not in self refresh mode (normal operating mode).
When this bit = 1b, the SDRAM is in self refresh mode.

bit 1 SDRAM Exit Self Refresh Trigger (Write Only)
This bit triggers the sequence that removes (exits) the SDRAM from Self Refresh mode.
Writing a 0b to this bit has no effect.
Writing a 1b to this bit triggers the exit self refresh sequence.

bit 0 SDRAM Enter Self Refresh Trigger (Write Only)
This bit triggers the sequence to places (enters) the SDRAM to Self Refresh mode.
Writing a 0b to this bit has no effect.
Writing a 1b to this bit triggers the enter self refresh sequence.

REG[0106h] SDRAM Refresh Clock Configuration Register
Default = 0177h Read/Write

SDRAM Refresh Clock Divide Select bits 15-8							
15	14	13	12	11	10	9	8
SDRAM Refresh Clock Divide Select bits 7-0							
7	6	5	4	3	2	0	0

bits 15-0 SDRAM Refresh Clock Divide Select bits [15:0]
These bits select the divide used to determine the SDRAM Refresh Clock frequency. These bits should be set such that the resulting refresh clock is approximately 64KHz. For further information on the clock structure, see Section Chapter 7, “Clocks” on page 45.

Refresh Clock Divide = REG[0106h] bits 15-0 + 1

The refresh clock is calculated using the following formula.

Refresh clock frequency = CLKI frequency ÷ Refresh Clock Divide

For example, the default register value of 0177h results in the following refresh frequency when CLKI is 24MHz.

Refresh clock frequency = 24MHz ÷ 375
= 64KHz

REG[0108h] SDRAM Read Data Tap Delay Select Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
n/a		SDRAM Read Data Sampling Select	SDRAM Read Data Sampling Clock Invert Enable	Reserved	Reserved		
7	6	5	4	3	2	1	0

bit 5 SDRAM Read Data Sampling Select
This bit selects when SDRAM read data is sampled.
When this bit = 0b, SDRAM read data is sampled on the positive edge.
When this bit = 1b, SDRAM read data is sampled on the negative edge.

bit 4 SDRAM Read Data Sampling Clock Invert Enable
This bit controls whether the sampling clock used for SDRAM data reads is inverted.
When this bit = 0b, the sampling clock is not inverted.
When this bit = 1b, the sampling clock is inverted.

bit 3 Reserved
This bit must be set to 0b.

bits 2-0 Reserved
These bits must be set to 000b.

REG[010Ah] SDRAM Extended Mode Configuration Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a	SDRAM Driver Strength bits 1-0		Temperature Compensated Self Refresh bits 1-0		Partial Array Self Refresh bits 2-0		

7	6	5	4	3	2	1	0
n/a					SDRAM Size bits 1-0		Extended Mode Register Program on Initialization Enable

bits 14-13 SDRAM Driver Strength bits [1:0]

These bits only have an effect when the Extended Mode Register Program On Initialization Enable bit is set to 1b, REG[010Ah] bit 0 = 1b. These bits set the value for Driver Strength (DS) that is programmed into the extended mode register of the mobile SDRAM.

Table 10-13 : SDRAM Driver Strength Selection

REG[010Ah] bits 14-13	Driver Strength
00b	Full Strength
01b	Half Strength
10b	Quarter Strength
11b	Eighth Strength

bits 12-11 Temperature Compensated Self Refresh bits [1:0]

These bits only have an effect when the Extended Mode Register Program On Initialization Enable bit is set to 1b, REG[010Ah] bit 0 = 1b. Mobile SDRAM allows the self refresh rate to be varied based on the temperature of the SDRAM. These bits set the value for Temperature Compensated Self Refresh (TCSR) that is programmed into the extended mode register of the mobile SDRAM.

bits 10-8 Partial Array Self Refresh bits [2:0]

These bits only have an effect when the Extended Mode Register Program On Initialization Enable bit is set to 1b, REG[010Ah] bit 0 = 1b. These bits set the value for Partial Array Self Refresh (PASR) that is programmed into the extended mode register of the mobile SDRAM.

bits 2-1 SDRAM Size bits [1:0]

These bits specify the SDRAM size, in M bytes. This setting is used for bank address placement.

Table 10-14 : SDRAM Size Selection

REG[010Ah] bits 2-1	SDRAM Size
00b	8M bytes
01b	16M bytes
10b	32M bytes
11b	64M bytes

bit 0 Extended Mode Register Program On Initialization Enable

When mobile SDRAM is used, this bit controls whether the extended mode register is programmed when the SDRAM is initialized, REG[0102h] bit 0 = 1b.

When this bit = 0b, the extended mode register is not programmed when the SDRAM is initialized.

When this bit = 1b, the extended mode register is programmed when the SDRAM is initialized.

REG[010Ch] SDRAM Controller Software Reset Register

Default = 0000h Write Only

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a							SDRAM Controller Software Reset

bit 0 SDRAM Controller Software Reset (Write Only)

This bit performs a software reset of the SDRAM controller.

Writing a 0b to this bit has no effect.

Writing a 1b to this bit performs a software reset of the SDRAM controller.

10.3.5 Host Interface Memory Access Configuration

REG[0140h] Host Memory Access Configuration and Status Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Host Memory Interface Reset (WO)	n/a	Host Memory Interface Ready Status (RO)	Host Memory Interface Busy Status (RO)	n/a		Write Rotation Select bits 1-0	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Packed Pixel Destination Start Address Select	n/a	Host Packed Pixel Select bits 1-0		Host Rotate 0 and 180 Line Buffer Bypass Enable	Memory Read/Write Select	Memory Access Type	

bit 15 Host Memory Interface Reset (Write Only)
This bit performs a software reset of the host memory interface.
Writing a 0b to this bit has no effect.
Writing a 1b to this bit initiates a software reset of the host memory interface.

bit 13 Host Memory Interface Ready Status (Read Only)
This bit indicates the ready status of the host memory interface once a data transfer has been triggered (see REG[0142h] bit 0).
When this bit = 0b, the host memory interface is not ready (busy filling or clearing the buffer).
When this bit = 1b, the host memory interface is ready for a data transfer.

bit 12 Host Memory Interface Busy Status (Read Only)
This bit indicates the busy status of the host memory interface.
When this bit = 0b, the host memory interface is idle.
When this bit = 1b, the host memory interface is busy.

bits 9-8 Write Rotation Select bits [1:0]
These bits only have an effect when Packed Pixel Access is selected, REG[0140h] bits 1-0 = 00b. These bits select the counter-clockwise rotation applied to host memory interface writes.

Table 10-15 : Write Rotation Selection

REG[0140h] bits 9-8	Write Rotation
00b	0°
01b	90°
10b	180°
11b	270°

bit 7 Packed Pixel Destination Start Address Select
When packed pixel mode is selected (REG[0140h] bits 1-0 = 00b), this bit determines the destination start address for the memory write.
When this bit = 0b, the destination start address is defined by the Display Engine image buffer start address, REG[0310h] ~ REG[0312h].
When this bit = 1b, the destination start address is defined by the Host raw memory access address, REG[0144h] ~ REG[0146h].

bits 5-4 Host Packed Pixel Select bits [1:0]

These bits only have an effect when Packed Pixel Access is selected, REG[0140h] bits 1-0 = 00b. These bits select the packed pixel mode used for host memory interface accesses.

Table 10-16 : Packed Pixel Mode Selection

REG[0140h] bits 5-4	Packed Pixel Mode
00b	2 bpp
01b	3 bpp
10b	4 bpp
11b	8 bpp

bit 3 Host Rotate 0 and 180 Line Buffer Bypass Enable

When the Write Rotation Select bits are set for 0° or 180° (REG[0140h] bits 9-8 = 00b or 10b), this bit determines whether the line buffer is used or bypassed. When write rotation is set for 90° or 270°, the line buffer is always used.

When this bit = 0b, the line buffer is used.

When this bit = 1b, the line buffer is bypassed (not used).

bit 2 Memory Read/Write Select

This bit selects the memory read/write direction.

When this bit = 0b, the host memory interface is configured to write to memory.

When this bit = 1b, the host memory interface is configured to read from memory.

bits 1-0 Memory Access Type Select bits [1:0]

These bits select the type of memory access performed through the host memory interface.

Table 10-17 : Memory Access Type Selection

REG[0140h] bits 1-0	Memory Access Type
00b	Packed Pixel Access (Write Only)
01b	Raw Memory Access (Read/Write)
10b ~ 11b	Reserved

REG[0142h] Host Memory Access Triggers Register

Default = 0000h Write Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	0	0
n/a						Host Transfer Stop Trigger	Host Transfer Start Trigger

bit 1 Host Transfer Stop Trigger (Write Only)

This bit stops the data transfer taking place on the host memory interface.

Writing a 0b to this bit has no effect.

Writing a 1b to this bit triggers the current host memory interface transfer to stop.

bit 0 Host Transfer Start Trigger (Write Only)

This bit starts a new data transfer on the host memory interface.

Writing a 0b to this bit has no effect.

Writing a 1b to this bit triggers a new data transfer to start on the host memory interface.

REG[0144h] Host Raw Memory Access Address Register 0
Default = 0000h Read/Write

Host Raw Memory Access Address bits 15-8							
15	14	13	12	11	10	9	8
Host Raw Memory Access Address bits 7-0							
7	6	5	4	3	2	0	0

REG[0146h] Host Raw Memory Access Address Register 1
Default = 0000h Read/Write

Host Raw Memory Access Address bits 31-24							
15	14	13	12	11	10	9	8
Host Raw Memory Access Address bits 23-16							
7	6	5	4	3	2	0	0

REG[0146h] bits 15-0
REG[0144h] bits 15-0 Host Raw Memory Access Address bits [31:0]
These bits are only used for raw memory accesses (REG[0104h] bits 1-0 = 01b). These bits specify the 32-bit memory address used for raw memory accesses by the host memory interface.

REG[0148h] Host Raw Memory Access Count Register 0
Default = 0000h Read/Write

Host Raw Memory Access Count bits 15-8							
15	14	13	12	11	10	9	8
Host Raw Memory Access Count bits 7-0							
7	6	5	4	3	2	0	0

REG[014Ah] Host Raw Memory Access 16-bit Access Count Register 1
Default = 0000h Read/Write

Host Raw Memory Access Count bits 31-24							
15	14	13	12	11	10	9	8
Host Raw Memory Access Count bits 23-16							
7	6	5	4	3	2	0	0

REG[014Ah] bits 15-0
REG[0148h] bits 15-0 Host Raw Memory Access Count bits [31:0]
These bits are only used for raw memory accesses (REG[0104h] bits 1-0 = 01b). These bits specify the number of 16-bit accesses that will be performed for raw memory accesses by the host memory interface during burst operations.

REG[014Ch] Packed Pixel Rectangular X-Start Register
Default = 0000h Read/Write

n/a			Packed Pixel Rectangular X-Start Position bits 12-8				
15	14	13	12	11	10	9	8
Packed Pixel Rectangular X-Start Position bits 7-0							
7	6	5	4	3	2	0	0

bits 12-0 Packed Pixel Rectangular X-Start Position bits [12:0]
These bits are only used for packed pixel accesses (REG[0104h] bits 1-0 = 00b). These bits specify the X-Start position of the image write, in pixels, relative to the top left corner of the display area. For further information, see Section 11.1, “Display Memory Area Setup” on page 150.

REG[014Eh] Packed Pixel Rectangular Y-Start Register
Default = 0000h Read/Write

n/a			Packed Pixel Rectangular Y-Start Position bits 12-8				
15	14	13	12	11	10	9	8
Packed Pixel Rectangular Y-Start Position bits 7-0							
7	6	5	4	3	2	0	0

bits 12-0 Packed Pixel Rectangular Y-Start Position bits [12:0]
These bits are only used for packed pixel accesses (REG[0104h] bits 1-0 = 00b). These bits specify the Y-Start position of the image write, in pixels, relative to the top left corner of the display area. For further information, see Section 11.1, “Display Memory Area Setup” on page 150.

REG[0150h] Packed Pixel Rectangular Width Register
Default = 0000h Read/Write

n/a			Packed Pixel Rectangular Width bits 12-8				
15	14	13	12	11	10	9	8
Packed Pixel Rectangular Width bits 7-0							
7	6	5	4	3	2	0	0

bits 12-0 Packed Pixel Rectangular Width bits [12:0]
These bits are only used for packed pixel accesses (REG[0104h] bits 1-0 = 00b). These bits specify the width of the image write, in pixels. For further information, see Section 11.1, “Display Memory Area Setup” on page 150.

REG[0152h] Packed Pixel Rectangular Height Register
Default = 0000h Read/Write

n/a			Packed Pixel Rectangular Height bits 12-8				
15	14	13	12	11	10	9	8
Packed Pixel Rectangular Height bits 7-0							
7	6	5	4	3	2	0	0

bits 12-0 Packed Pixel Rectangular Height bits [12:0]
These bits are only used for packed pixel accesses (REG[0104h] bits 1-0 = 00b). These bits specify the height of the image write, in pixels. For further information, see Section 11.1, “Display Memory Area Setup” on page 150.

REG[0154h] Host Memory Access Port Register
Default = 0000h — Read/Write

Host Memory Access Port bits 15-8							
15	14	13	12	11	10	9	8
Host Memory Access Port bits 7-0							
7	6	5	4	3	2	0	0

bits 15-0 Host Memory Access Port bits [15:0]
These bits are the data port for host memory interface accesses.

REG[0156h] Host Memory Checksum Register
Default = 0000h — Read/Write

Host Memory Checksum bits 15-8							
15	14	13	12	11	10	9	8
Host Memory Checksum bits 7-0							
7	6	5	4	3	2	0	0

bits 15-0 Host Memory Checksum bits [15:0]
These bits contain a checksum value of all 16-bit memory accesses. After each 16-bit memory access, the data value is added to the value in this register.

To reset the checksum calculation, the Host must write 00h to these bits.

10.3.6 SPI Flash Memory Interface

REG[0200h] SPI Flash Read Data Register
Default = 0000h — Read Only

15	14	13	12	11	10	9	8
n/a							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SPI Flash Read Data bits 7-0							

bits 7-0 SPI Flash Read Data bits [7:0] (Read Only)
These bits contain the 8-bit data value received from the SPI Flash Memory. A read data transfer is triggered by a "dummy" write to REG[0202h] where bit 8 = 0b.

REG[0202h] SPI Flash Write Data Register
Default = 0000h — Write Only

15	14	13	12	11	10	9	8
n/a							SPI Flash Data Output Enable
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SPI Flash Write Data bits 7-0							

bit 8 SPI Flash Data Output Enable (Write Only)
This bit determines whether a read or write data transfer takes place on the SPI Flash Memory interface.
When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer is triggered by a "dummy" write to REG[0202h].
When this bit = 1b, a write data transfer to the SPI Flash Memory takes place.

bits 7-0 SPI Flash Write Data bits [7:0] (Write Only)
These bits are the write data register for the SPI Flash Memory. A write data transfer is triggered by a write to REG[0202h] where bit 8 = 1b. When the status flag for this register shows empty, the CPU is permitted to write data into this register.

REG[0204h] SPI Flash Control Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							
SPI Flash Access Mode Select	SPI Flash Read Command Select	SPI Flash Clock Divide Select bits 2-0			SPI Flash Clock Phase Select	SPI Flash Clock Polarity Select	SPI Flash Enable
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**

bit 7 SPI Flash Access Mode Select
This bit selects between Display Engine access mode and Host Register access mode. This bit must be set to 1b before performing a Display Engine operation to allow the Display Engine to communicate with SPI Flash Memory.
When this bit = 0b, Host Register access mode is selected.
When this bit = 1b, Display Engine access mode is selected.

bit 6 SPI Flash Read Command Select

This bit selects which serial flash command is used for reading data and depends on the SPI Flash Memory device. Please refer to the device data sheet to determine which setting is appropriate.

When this bit = 0b, the serial flash read speed is Low.

When this bit = 1b, the serial flash read speed is High.

bits 5-3 SPI Flash Clock Divide Select bits [2:0]

These bits select the divide ratio for the SPI Flash Clock which is derived from either the PLL output or CLKI depending on the setting of the PLL Bypass Mode Enable bit, REG[0016h] bit 0. For further details on the clock structure, see Section Chapter 7, “Clocks” on page 45.

Table 10-18: SPI Flash Clock Divide Ratio Selection

REG[0204h] bits 5-3	SPI Flash Clock Divide Ratio	REG[0204h] bits 5-3	SPI Flash Clock Divide Ratio
000b	1:2	100b	1:6
001b	1:3	101b	1:7
010b	1:4	110b	1:8
011b	1:5	111b	1:9

bit 2 SPI Flash Clock Phase Select

This bit selects the SPI Flash clock phase. For a summary of the SPI Flash Memory clock phase and polarity settings, see Table 10-19 “SPI Flash Clock Phase and Polarity,” on page 100.

bit 1 SPI Flash Clock Polarity Select (CPOL)

This bit selects the SPI Flash clock polarity. The following table summarizes the SPI Flash clock polarity and phase settings.

Table 10-19 : SPI Flash Clock Phase and Polarity

REG[0204h] bit 2	REG[0204h] bit 1	Valid Data	Clock Idling Status
0b	0b	Rising edge of SPI Flash Clock	Low
	1b	Falling edge of SPI Flash Clock	High
1b	0b	Falling edge of SPI Flash Clock	Low
	1b	Rising edge of SPI Flash Clock	High

bit 0 SPI Flash Enable

This bit controls the SPI Flash Memory interface logic.

When this bit = 0b, the SPI Flash Memory interface is disabled.

When this bit = 1b, the SPI Flash Memory interface is enabled.

Note

The SPI Flash Memory interface should be disabled (REG[0204h] bit 0 = 0b) before programming the SPI Flash registers, REG[0200h] ~ REG[0208h].

REG[0206h] SPI Flash Status Register

Default = 0004h — Read Only

n/a							
15	14	13	12	11	10	9	8
n/a				SPI Flash Busy Flag	SPI Flash Write Data Register Empty Flag	SPI Flash Read Data Overrun Flag	SPI Flash Read Data Ready Flag
7	6	5	4	3	2	1	0

bit 3 SPI Flash Busy Flag (Read Only)
This bit indicates the status of the SPI Flash Memory interface.
When this bit = 0b, the SPI Flash Memory interface is not busy (idle).
When this bit = 1b, the SPI Flash Memory interface is busy.

bit 2 SPI Flash Write Data Register Empty Flag (Read Only)
This bit indicates when the SPI Flash Write Data register (REG[0202h]) is empty which occurs when data written to the register is latched for serialization/transmission.
When this bit = 0b, the SPI Flash Write Data register is not empty.
When this bit = 1b, the SPI Flash Write Data register is empty. (default)

To clear this flag, write data to the SPI Flash Write Data register, REG[0202h].

bit 1 SPI Flash Read Data Overrun Flag (Read Only)
This bit indicates when new data is loaded into the SPI Flash Read Data register (REG[0200h]) before the existing data has been read (REG[0206h] bit 0 = 1b while the new data is loaded). In this case, the old data is no longer available and must be re-read.
When this bit = 0b, a SPI Flash Read Data overrun has not occurred.
When this bit = 1b, a SPI Flash Read Data overrun has occurred.

To clear this flag, read the SPI Flash Read Data register, REG[0200h].

bit 0 SPI Flash Read Data Ready Flag (Read Only)
This bit indicates when read data from the SPI Flash Memory is available (or ready) in the SPI Flash Read Data register, REG[0200h].
When this bit = 0b, the SPI Flash Memory read data is not ready.
When this bit = 1b, the SPI Flash Memory read data is ready.

To clear this flag, read the SPI Flash Read Data register, REG[0200h].

REG[0208h] SPI Flash Chip Select Control Register

Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a							SPI Flash Chip Select Enable

bit 0 SPI Flash Chip Select Enable

This bit controls chip select (SPIDCS_L) for the SPI Flash Memory interface and is used to access the serial EEPROM.

When this bit = 0b, the chip select for the slave device is disabled.

When this bit = 1b, the chip select for the slave device is enabled.

Note

The chip select output pin for the Serial Flash Memory interface is active low. Therefore, SPIDCS_L is high when this bit = 0b, and SPIDCS_L is low when this bit = 1b.

10.3.7 I2C Thermal Sensor Interface Registers

REG[0210h] I2C Thermal Sensor Configuration Register
Default = 0000h — Read/Write

n/a					I2C Thermal Sensor ID Address bits 2-0		
15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0

bits 10-8 I2C Thermal Sensor ID Address bits [2:0]
These bits are the three least significant bits of the I2C thermal sensor ID address, A[2:0]. A[6:3] are fixed to a value of 1001b. The default value for A[2:0] is 000b, resulting in a default ID address of 100_1000b (48h).

REG[0212h] I2C Thermal Sensor Status Register
Default = 0006h — Read Only

n/a							
15	14	13	12	11	10	9	8
n/a		I2C SDA Pin Status	I2C SCL Pin Status	n/a	I2C Thermal Sensor Data Status	I2C Thermal Sensor ID Status	I2C Thermal Sensor Busy Status
7	6	5	4	3	2	1	0

bit 5 I2C SDA Pin Status (Read Only)
This bit indicates the status of the I2C SDA pin which is used to communicate with the Thermal Sensor.
When this bit = 0b, the I2C SDA pin is low (0).
When this bit = 1b, the I2C SDA pin is high (1).

bit 4 I2C SCL Pin Status (Read Only)
This bit indicates the status of the I2C SCL pin which is used to communicate with the Thermal Sensor.
When this bit = 0b, the I2C SCL pin is low (0).
When this bit = 1b, the I2C SCL pin is high (1).

bit 2 I2C Thermal Sensor Data Status (Read Only)
This bit indicates the status of temperature value data returned from the Thermal Sensor.
When this bit = 0b, temperature value data has been returned from the thermal sensor (ACK).
When this bit = 1b, temperature value data has not been returned from the thermal sensor (NACK).

bit 1 I2C Thermal Sensor ID Status (Read Only)
This bit indicates the status of the Thermal Sensor ID transfer.
When this bit = 0b, the thermal sensor ID has been transferred (ACK).
When this bit = 1b, the thermal sensor ID has not been transferred (NACK).

bit 0 I2C Thermal Sensor Busy Status (Read Only)
This bit indicates the status of the I2C Thermal Sensor.
When this bit = 0b, the I2C thermal sensor is idle (not busy).
When this bit = 1b, the I2C thermal sensor is busy.

REG[0214h] I2C Thermal Sensor Read Trigger Register

Default = 0007h — Write Only

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
n/a							I2C Thermal Sensor Read Trigger

bit 0 — I2C Thermal Sensor Read Trigger (Write Only)

This bit triggers the thermal sensor to read the current temperature which is stored in the I2C Thermal Sensor Temperature Value register, REG[0216h].

Writing a 0b to this bit has no effect.

Writing a 1b to this bit triggers a temperature read from the Thermal Sensor.

REG[0216h] I2C Thermal Sensor Temperature Value Register

Default = 0007h — Read Only

15	14	13	12	11	10	9	8
n/a							

7	6	5	4	3	2	1	0
I2C Thermal Sensor Temperature Value bits 7-0							

bits 7-0 — I2C Thermal Sensor Temperature Value bits [7:0] (Read Only)

These bits indicate the temperature value received from the I2C Thermal Sensor after a I2C thermal sensor read has been triggered, REG[0214h] bit 0 = 1b. The temperature value is stored in 2's compliment format.

10.3.8 3-Wire Chip Interface Registers

REG[0220h] 3-Wire Chip Configuration Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a							3-Wire Chip Read/Write Select
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
n/a			3-Wire Chip Interface Clock Divide Select bits 4-0				

bit 8 — 3-Wire Chip Read/Write Select
This bit selects whether a read or write operation is performed from/to the 3-Wire chip. A read/write operation is triggered by a write to the 3-Wire Chip Address bits, REG[0224h] bits 7-0.
When this bit = 0b, a write operation is selected (see REG[0224h] bits 15-8).
When this bit = 1b, a read operation is selected (see REG[0226h] bits 7-0).

bits 4-0 — 3-Wire Chip Interface Clock Divide Select bits [4:0]
These bits select the divide ratio used to generate the clock for the 3-Wire Chip interface. The clock is derived from either the PLL output or CLKI depending on the setting of the PLL Bypass Mode Enable bit, REG[0016h] bit 0. For further details on the clock structure, see Section Chapter 7, “Clocks” on page 45.

Table 10-20: 3-Wire Chip Interface Clock Divide Selection

REG[0200h] bits 4-0	Divide Ratio
0_0000b (00h)	1:2
0_0001b (01h)	1:4
0_0010b (02h)	1:8
0_0011b (03h)	1:16
0_0100b ~ 1_1111b (04h ~ 1Fh)	Reserved

REG[0222h] 3-Wire Chip Access Status Register
Default = 0000h — Read Only

15	14	13	12	11	10	9	8
n/a							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
n/a					3-Wire Chip Data Byte Transfer Status	3-Wire Chip Address Byte Send Status	3-Wire Chip Operation Status

bit 2 — 3-Wire Chip Data Byte Transfer Status (Read Only)
This bit indicates the status of the data byte transfer (send/receive) on the 3-Wire Chip interface.
When this bit = 0b, a data byte is not being transferred (not busy).
When this bit = 1b, a data byte is being transferred (busy).

bit 1 — 3-Wire Chip Address Byte Send Status (Read Only)
This bit indicates the status of the address byte transfer (send) on the 3-Wire Chip interface.
When this bit = 0b, an address byte is not being transferred (not busy).
When this bit = 1b, an address byte is being transferred (busy).

bit 0 3-Wire Chip Operation Status (Read Only)
This bit indicates the status of the 3-wire chip interface.
When this bit = 0b, the 3-wire chip interface is idle (not busy).
When this bit = 1b, the 3-wire chip interface is busy.

REG[0224h] 3-Wire Chip Address and Write Data Byte Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
3-Wire Chip Write Data bits 7-0							
7	6	5	4	3	2	1	0
3-Wire Chip Address bits 7-0							

bits 15-8 3-Wire Chip Write Data bits [7:0]
These bits specify the data to be written to the 3-Wire Chip during a write operation (REG[0220h] bit 8 = 0b). These bits are not used if a read operation is selected.

bits 7-0 3-Wire Chip Address bits [7:0]
These bits specify the address for the transfer to or from the 3-Wire Chip. A transfer is triggered by a write to these bits.

REG[0226h] 3-Wire Chip Read Data Byte Register
Default = 0000h Read Only

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
3-Wire Chip Read Data bits 7-0							

bits 7-0 3-Wire Chip Read Data bits [7:0] (Read Only)
These bits return the data read from the 3-Wire Chip in the previous read operation (REG[0220h] bit 8 = 1b).

10.3.9 Power Pin Control Configuration Registers

Power Pin control uses the PWR[3:0] pins which can be programmed to perform a power-on/off cycle using the Power Pin Timing Delay registers (REG[0234h] ~ REG[0238h]) and the PWRCOM pin which is controlled by the Display Engine. Both PWR[3:0] and PWRCOM can be manually controlled using the bypass option (see REG[0232h]).

REG[0230h] Power Pin Control Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a			PWR3 Pin Status (RO)	PWR2 Pin Status (RO)	PWR1 Pin Status (RO)	PWR0 Pin Status (RO)	PWRCOM Pin Status (RO)
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Power Cycle Busy (RO)	n/a					Power-Off Cycle Trigger (WO)	Power-On Cycle Trigger (WO)

bits 12-9 PWR[3:0] Pin Status (Read Only)
These bits indicates the status of the individual PWR[3:0] pins.
When this bit = 0b, the PWR[3:0] pin is low (0).
When this bit = 1b, the PWR[3:0] pin is high (1).

bit 8 PWRCOM Pin Status (Read Only)
This bit indicates the status of the PWRCOM pin.
When this bit = 0b, the PWRCOM pin is low (0).
When this bit = 1b, the PWRCOM pin is high (1).

bit 7 Power Cycle Busy (Read Only)
This bit indicates whether a power-on/off cycle is currently happening.
When this bit = 0b, a power-on/off cycle is not happening (not busy).
When this bit = 1b, a power-on/off cycle is happening (busy).

bit 1 Power-Off Cycle Trigger (Write Only)
This bit triggers a power-off cycle on the PWR[3:0] pins. Before triggering a power-off cycle, the power pin delay times should be configured using the Power Pin Timing Delay registers, REG[0234h] ~ REG[0238h].
Writing a 0b to this bit has no effect.
Writing a 1b to this bit triggers a a power-off cycle on the PWR[3:0] pins.

bit 0 Power-On Cycle Trigger (Write Only)
This bit triggers a power-on cycle on the PWR[3:0] pins. Before triggering a power-on cycle, the power pin delay times should be configured using the Power Pin Timing Delay registers, REG[0234h] ~ REG[0238h].
Writing a 0b to this bit has no effect.
Writing a 1b to this bit triggers a a power-on cycle on the PWR[3:0] pins.

REG[0232h] Power Pin Configuration Register
Default = 0000h Read/Write

n/a			PWR3 Pin Bypass Enable	PWR2 Pin Bypass Enable	PWR1 Pin Bypass Enable	PWR0 Pin Bypass Enable	PWRCOM Pin Bypass Enable
15	14	13	12	11	10	9	8
n/a			PWR3 Pin Bypass Value	PWR2 Pin Bypass Value	PWR1 Pin Bypass Value	PWR0 Pin Bypass Value	PWRCOM Pin Bypass Value
7	6	5	4	3	2	1	0

bit 12 PWR3 Pin Bypass Enable
This bit controls PWR3 pin bypass mode which allows the PWR3 pin output value to be set directly. When bypass mode is enabled, the Trigger bits (REG[0230h] bits 1-0) and the Timing Delay bits (REG[0234] ~ REG[0238h]) have no effect.
When this bit = 0b, PWR3 pin bypass mode is disabled.
When this bit = 1b, PWR3 pin bypass mode is enabled and the PWR3 pin output is set to the value specified by the PWR3 Pin Bypass Value, REG[0232h] bit 4.

bit 11 PWR2 Pin Bypass Enable
This bit controls PWR2 pin bypass mode which allows the PWR2 pin output value to be set directly. When bypass mode is enabled, the Trigger bits (REG[0230h] bits 1-0) and the Timing Delay bits (REG[0234] ~ REG[0238h]) have no effect.
When this bit = 0b, PWR2 pin bypass mode is disabled.
When this bit = 1b, PWR2 pin bypass mode is enabled and the PWR2 pin output is set to the value specified by the PWR2 Pin Bypass Value, REG[0232h] bit 3.

bit 10 PWR1 Pin Bypass Enable
This bit controls PWR1 pin bypass mode which allows the PWR1 pin output value to be set directly. When bypass mode is enabled, the Trigger bits (REG[0230h] bits 1-0) and the Timing Delay bits (REG[0234] ~ REG[0238h]) have no effect.
When this bit = 0b, PWR1 pin bypass mode is disabled.
When this bit = 1b, PWR1 pin bypass mode is enabled and the PWR1 pin output is set to the value specified by the PWR1 Pin Bypass Value, REG[0232h] bit 2.

bit 9 PWR0 Pin Bypass Enable
This bit controls PWR0 pin bypass mode which allows the PWR0 pin output value to be set directly. When bypass mode is enabled, the Trigger bits (REG[0230h] bits 1-0) and the Timing Delay bits (REG[0234] ~ REG[0238h]) have no effect.
When this bit = 0b, PWR0 pin bypass mode is disabled.
When this bit = 1b, PWR0 pin bypass mode is enabled and the PWR0 pin output is set to the value specified by the PWR0 Pin Bypass Value, REG[0232h] bit 1.

bit 8 PWRCOM Pin Bypass Enable
This bit controls PWRCOM pin bypass mode which allows the PWRCOM pin output value to be set directly. When bypass mode is enabled, the Trigger bits (REG[0230h] bits 1-0) and the Timing Delay bits (REG[0234] ~ REG[0238h]) have no effect.
When this bit = 0b, PWRCOM pin bypass mode is disabled.
When this bit = 1b, PWRCOM pin bypass mode is enabled and the PWRCOM pin output is set to the value specified by the PWRCOM Pin Bypass Value, REG[0232h] bit 0.

bit 4 PWR3 Pin Bypass Value
When the PWR3 Pin Bypass Enable bit is set (REG[0232h] bit 12 = 1b), this bit specifies the value that is output on the PWR3 pin.
When this bit = 0b, a 0 is output on the PWR3 pin (low).
When this bit = 1b, a 1 is output on the PWR3 pin (high).

bit 3 PWR2 Pin Bypass Value
When the PWR2 Pin Bypass Enable bit is set (REG[0232h] bit 11 = 1b), this bit specifies the value that is output on the PWR2 pin.
When this bit = 0b, a 0 is output on the PWR2 pin (low).
When this bit = 1b, a 1 is output on the PWR2 pin (high).

bit 2 PWR1 Pin Bypass Value
When the PWR1 Pin Bypass Enable bit is set (REG[0232h] bit 10 = 1b), this bit specifies the value that is output on the PWR1 pin.
When this bit = 0b, a 0 is output on the PWR1 pin (low).
When this bit = 1b, a 1 is output on the PWR1 pin (high).

bit 1 PWR0 Pin Bypass Value
When the PWR0 Pin Bypass Enable bit is set (REG[0232h] bit 9 = 1b), this bit specifies the value that is output on the PWR0 pin.
When this bit = 0b, a 0 is output on the PWR0 pin (low).
When this bit = 1b, a 1 is output on the PWR0 pin (high).

bit 0 PWRCOM Pin Bypass Value
When the PWRCOM Pin Bypass Enable bit is set (REG[0232h] bit 8 = 1b), this bit specifies the value that is output on the PWRCOM pin.
When this bit = 0b, a 0 is output on the PWRCOM pin (low).
When this bit = 1b, a 1 is output on the PWRCOM pin (high).

REG[0234h] Power Pin Timing Delay 0-1 Register
Default = 0000h Read/Write

n/a				Power Pin Timing Delay 0-1 bits 11-8			
15	14	13	12	11	10	9	8
Power Pin Timing Delay 0-1 bits 7-0							
7	6	5	4	3	2	1	0

bits 11-0 Power Pin Timing Delay 0-1 bits [11:0]
These bits specify the delay timing between PWR0 pin and PWR1 pin changes. For timing details, refer to Section 6.6.1, “Power Pin Transition Sequence for PWR[3:0]” on page 43.
Delay time = ((REG[0234h] bits 11-0) ÷ 16) - 1

REG[0236h] Power Pin Timing Delay 1-2 Register
Default = 0000h Read/Write

n/a				Power Pin Timing Delay 1-2 bits 11-8			
15	14	13	12	11	10	9	8
Power Pin Timing Delay 1-2 bits 7-0							
7	6	5	4	3	2	1	0

bits 11-0 Power Pin Timing Delay 1-2 bits [11:0]
These bits specify the delay timing between PWR1 pin and PWR2 pin changes. For timing details, refer to Section 6.6.1, “Power Pin Transition Sequence for PWR[3:0]” on page 43.
Delay time = ((REG[0236h] bits 11-0) ÷ 16) - 1

REG[0238h] Power Pin Timing Delay 2-3 Register
Default = 0000h Read/Write

n/a				Power Pin Timing Delay 2-3 bits 11-8			
15	14	13	12	11	10	9	8
Power Pin Timing Delay 2-3 bits 7-0							
7	6	5	4	3	2	1	0

bits 11-0 Power Pin Timing Delay 2-3 bits [11:0]
These bits specify the delay timing between PWR2 pin and PWR3 pin changes. For timing details, refer to Section 6.6.1, “Power Pin Transition Sequence for PWR[3:0]” on page 43.
Delay time = ((REG[0238h] bits 11-0) ÷ 16) - 1

10.3.10 Interrupt Configuration Registers

REG[0240h] Interrupt Raw Status Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						Reserved	Host Memory Read/Write FIFO Error Interrupt Raw Status
7	6	5	4	3	2	1	0
SDRAM Self Refresh Enter/Exit Interrupt Raw Status	I2C Thermal Sensor Read Done Interrupt Raw Status	Power Management Controller Interrupt Raw Status	3-Wire Chip Interrupt Raw Status	GPIO Interrupt Raw Status	Host Memory Transfer Complete Interrupt Raw Status	Display Engine Interrupt Raw Status	SDRAM Initialization Complete Interrupt Raw Status

bit 9 Reserved
The default value for this bit is 0b.

bit 8 Host Memory Read/Write FIFO Error Interrupt Raw Status
This bit indicates the raw status of the Host Memory Read/Write FIFO Error Interrupt and is not masked by the Host Memory Read/Write FIFO Error Interrupt Enable bit, REG[0244h] bit 8.
When this bit = 0b, a Host Memory Read/Write FIFO Error Interrupt has not occurred.
When this bit = 1b, a Host Memory Read/Write FIFO Error Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0242h] bit 8.

bit 7 SDRAM Self Refresh Enter/Exit Interrupt Raw Status
This bit indicates the raw status of the SDRAM Self Refresh Enter/Exit Interrupt and is not masked by the SDRAM Self Refresh Enter/Exit Interrupt Enable bit, REG[0244h] bit 7.
When this bit = 0b, a SDRAM Self Refresh Enter/Exit Interrupt has not occurred.
When this bit = 1b, a SDRAM Self Refresh Enter/Exit Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0242h] bit 7.

bit 6 I2C Thermal Sensor Read Done Interrupt Raw Status
This bit indicates the raw status of the I2C Thermal Sensor Read Done Interrupt and is not masked by the I2C Thermal Sensor Read Done Interrupt Enable bit, REG[0244h] bit 6.
When this bit = 0b, an I2C Thermal Sensor Read Done Interrupt has not occurred.
When this bit = 1b, an I2C Thermal Sensor Read Done Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0242h] bit 6.

bit 5 Power Management Controller Interrupt Raw Status
This bit indicates the raw status of the Power Management Controller Interrupt and is not masked by the Power Management Controller Interrupt Enable bit, REG[0244h] bit 5.
When this bit = 0b, a Power Management Controller Interrupt has not occurred.
When this bit = 1b, a Power Management Controller Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0242h] bit 5.

bit 4	3-Wire Chip Interrupt Raw Status This bit indicates the raw status of the 3-Wire Chip Interrupt and is not masked by the 3-Wire Chip Interrupt Enable bit, REG[0244h] bit 4. When this bit = 0b, a 3-Wire Chip Interrupt has not occurred. When this bit = 1b, a 3-Wire Chip Interrupt has occurred. To clear this status bit, write a 1b to either this bit or REG[0242h] bit 4.
bit 3	GPIO Interrupt Raw Status This bit indicates the raw status of the GPIO Interrupt and is not masked by the GPIO Interrupt Enable bit, REG[0244h] bit 3. When this bit = 0b, a GPIO Interrupt has not occurred. When this bit = 1b, a GPIO Interrupt has occurred. To clear this status bit, write a 1b to either this bit or REG[0242h] bit 3.
bit 2	Host Memory Transfer Complete Interrupt Raw Status This bit indicates the raw status of the Host Memory Transfer Complete Interrupt and is not masked by the Host Memory Transfer Complete Interrupt Enable bit, REG[0244h] bit 2. When this bit = 0b, a Host Memory Transfer Complete Interrupt has not occurred. When this bit = 1b, a Host Memory Transfer Complete Interrupt has occurred. To clear this status bit, write a 1b to either this bit or REG[0242h] bit 2.
bit 1	Display Engine Interrupt Raw Status This bit indicates the raw status of the Display Engine Interrupt which occurs when one of the interrupts in REG[033Ah] or REG[033Ch] is triggered. This bit is not masked by the Display Engine Interrupt Enable bit, REG[0244h] bit 1. When this bit = 0b, a Display Engine Interrupt has not occurred. When this bit = 1b, a Display Engine Interrupt has occurred. To clear this status bit, clear the triggering interrupt in REG[033Ah] or REG[033Ch].
bit 0	SDRAM Initialization Complete Interrupt Raw Status This bit indicates the raw status of the SDRAM Initialization Complete Interrupt and is not masked by the SDRAM Initialization Complete Interrupt Enable bit, REG[0244h] bit 0. When this bit = 0b, a SDRAM Initialization Complete Interrupt has not occurred. When this bit = 1b, a SDRAM Initialization Complete Interrupt has occurred. To clear this status bit, write a 1b to either this bit or REG[0242h] bit 0.

REG[0242h] Interrupt Masked Status Register
Default = 0000h Read/Write

n/a						Reserved	Host Memory Read/Write FIFO Error Interrupt Masked Status
15	14	13	12	11	10	9	8
SDRAM Self Refresh Enter/Exit Interrupt Masked Status	I2C Thermal Sensor Read Done Interrupt Masked Status	Power Management Controller Interrupt Masked Status	3-Wire Chip Interrupt Masked Status	GPIO Interrupt Masked Status	Host Memory Transfer Complete Interrupt Masked Status	Display Engine Interrupt Masked Status	SDRAM Initialization Complete Interrupt Masked Status
7	6	5	4	3	2	1	0

bit 9 Reserved
The default value for this bit is 0b.

bit 8 Host Memory Read/Write FIFO Error Interrupt Masked Status
This bit indicates the masked status of the Host Memory Read/Write FIFO Error Interrupt (see REG[0244h] bit 8).
When this bit = 0b, a Host Memory Read/Write FIFO Error Interrupt has not occurred.
When this bit = 1b, a Host Memory Read/Write FIFO Error Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0240h] bit 8.

bit 7 SDRAM Self Refresh Enter/Exit Interrupt Masked Status
This bit indicates the masked status of the SDRAM Self Refresh Enter/Exit Interrupt (see REG[0244h] bit 7).
When this bit = 0b, a SDRAM Self Refresh Enter/Exit Interrupt has not occurred.
When this bit = 1b, a SDRAM Self Refresh Enter/Exit Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0240h] bit 7.

bit 6 I2C Thermal Sensor Read Done Interrupt Masked Status
This bit indicates the masked status of the I2C Thermal Sensor Read Done Interrupt (see REG[0244h] bit 6).
When this bit = 0b, an I2C Thermal Sensor Read Done Interrupt has not occurred.
When this bit = 1b, an I2C Thermal Sensor Read Done Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0240h] bit 6.

bit 5 Power Management Controller Interrupt Masked Status
This bit indicates the masked status of the Power Management Controller Interrupt (see REG[0244h] bit 5).
When this bit = 0b, a Power Management Controller Interrupt has not occurred.
When this bit = 1b, a Power Management Controller Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[0240h] bit 5.

bit 4	3-Wire Chip Interrupt Masked Status This bit indicates the masked status of the 3-Wire Chip Interrupt (see REG[0244h] bit 4). When this bit = 0b, a 3-Wire Chip Interrupt has not occurred. When this bit = 1b, a 3-Wire Chip Interrupt has occurred. To clear this status bit, write a 1b to either this bit or REG[0240h] bit 4.
bit 3	GPIO Interrupt Masked Status This bit indicates the masked status of the GPIO Interrupt (see REG[0244h] bit 3). When this bit = 0b, a GPIO Interrupt has not occurred. When this bit = 1b, a GPIO Interrupt has occurred. To clear this status bit, write a 1b to either this bit or REG[0240h] bit 3.
bit 2	Host Memory Transfer Complete Interrupt Masked Status This bit indicates the masked status of the Host Memory Transfer Complete Interrupt (see REG[0244h] bit 2). When this bit = 0b, a Host Memory Transfer Complete Interrupt has not occurred. When this bit = 1b, a Host Memory Transfer Complete Interrupt has occurred. To clear this status bit, write a 1b to either this bit or REG[0240h] bit 2.
bit 1	Display Engine Interrupt Masked Status This bit indicates the masked status of the Display Engine Interrupt (see REG[0244h] bit 1) which occurs when one of the interrupts in REG[033Ah] or REG[033Ch] is triggered. When this bit = 0b, a Display Engine Interrupt has not occurred. When this bit = 1b, a Display Engine Interrupt has occurred. To clear this status bit, clear the triggering interrupt in REG[033Ah] or REG[033Ch].
bit 0	SDRAM Initialization Complete Interrupt Masked Status This bit indicates the masked status of the SDRAM Initialization Complete Interrupt (see REG[0244h] bit 0). When this bit = 0b, a SDRAM Initialization Complete Interrupt has not occurred. When this bit = 1b, a SDRAM Initialization Complete Interrupt has occurred. To clear this status bit, write a 1b to either this bit or REG[0240h] bit 0.

REG[0244h] Interrupt Control Register
Default = 0000h Read/Write

n/a						Reserved	Host Memory Read/Write FIFO Error Interrupt Enable
15	14	13	12	11	10	9	8
SDRAM Self Refresh Enter/Exit Interrupt Enable	I2C Thermal Sensor Read Done Interrupt Enable	Power Management Controller Interrupt Enable	3-Wire Chip Interrupt Enable	GPIO Interrupt Enable	Host Memory Transfer Complete Interrupt Enable	Display Engine Interrupt Enable	SDRAM Initialization Complete Interrupt Enable
7	6	5	4	3	2	1	0

bit 9 Reserved
The default value for this bit is 0b.

bit 8 Host Memory Read/Write FIFO Error Interrupt Enable
This bit controls whether the Host Memory Read/Write FIFO Error Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 8 (unmasked) or REG[0242h] bit 8 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 7 SDRAM Self Refresh Enter/Exit Interrupt Enable
This bit controls whether the SDRAM Self Refresh Enter/Exit Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 7 (unmasked) or REG[0242h] bit 7 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 6 I2C Thermal Sensor Read Done Interrupt Enable
This bit controls whether the I2C Thermal Sensor Read Done Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 6 (unmasked) or REG[0242h] bit 6 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 5 Power Management Controller Interrupt Enable
This bit controls whether the Power Management Controller Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 5 (unmasked) or REG[0242h] bit 5 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 4 3-Wire Chip Interrupt Enable
This bit controls whether the 3-Wire Chip Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 4 (unmasked) or REG[0242h] bit 4 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 3	GPIO Interrupt Enable This bit controls whether the GPIO Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 3 (unmasked) or REG[0242h] bit 3 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 2	Host Memory Transfer Complete Interrupt Enable This bit controls whether the Host Memory Transfer Complete Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 2 (unmasked) or REG[0242h] bit 2 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 1	Display Engine Interrupt Enable This bit controls whether the Display Engine Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 1 (unmasked) or REG[0242h] bit 1 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 0	SDRAM Initialization Complete Interrupt Enable This bit controls whether the SDRAM Initialization Complete Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 0 (unmasked) or REG[0242h] bit 0 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.

10.3.11 GPIO Control Registers

REG[0250h] GPIO Configuration Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						GPIO1 Pull-down Control	GPIO0 Pull-down Control
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
n/a						GPIO1 Configuration	GPIO0 Configuration

bits 9-8 GPIO[1:0] Pull-down Control
All GPIO pins have internal pull-down resistors. These bits control the state of the pull-down resistor for each GPIOx pin.
When the bit = 0b, the pull-down resistor for the corresponding GPIOx pin is inactive. (default)
When the bit = 1b, the pull-down resistor for the corresponding GPIO pin is active.

bits 1-0 GPIO[1:0] Configuration
These bits configure each individual GPIO pin between an input or an output.
When this bit = 0b, the corresponding GPIO pin is configured as an input pin. (default)
When this bit = 1b, the corresponding GPIO pin is configured as an output pin.

REG[0252h] GPIO Status/Control Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						GPIO1 Input Status (RO)	GPIO0 Input Status (RO)
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
n/a						GPIO1 Data Output Control	GPIO0 Data Output Control

bits 9-8 GPIO[1:0] Input Status (Read Only)
When GPIOx is configured as an input (see REG[0250h] bits 1-0), a read from this bit returns the state of the corresponding GPIOx pin.
When this bit = 0b, the GPIOx pin is 0 (low).
When this bit = 1b, the GPIOx pin is 1 (high).

bits 1-0 GPIO[1:0] Data Output Control
When GPIOx is configured as an output (see REG[0250h] bits 1-0), a write to this bit drives the output state of the corresponding GPIOx pin.
When this bit = 0b, the corresponding GPIOx pin is driven to 0 (low). (default)
When this bit = 1b, the corresponding GPIOx pin is driven to 1 (high).

REG[0254h] GPIO Interrupt Enable Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						GPIO1 Negative Edge Interrupt Enable	GPIO0 Negative Edge Interrupt Enable
7	6	5	4	3	2	1	0
n/a						GPIO1 Positive Edge Interrupt Enable	GPIO0 Positive Edge Interrupt Enable

bits 9-8 GPIO[1:0] Negative Edge Interrupt Enable
These bits control whether the corresponding GPIOx interrupt (see REG[0256h]) is triggered on the negative edge (when the GPIOx pin changes from 1 to 0).
When this bit = 0b, the corresponding GPIOx interrupt is not triggered on the negative edge. (default)
When this bit = 1b, the corresponding GPIOx interrupt is triggered on the negative edge.

bits 1-0 GPIO[1:0] Positive Edge Interrupt Enable
These bits control whether the corresponding GPIOx interrupt (see REG[0256h]) is triggered on the positive edge (when the GPIOx pin changes from 0 to 1).
When this bit = 0b, the corresponding GPIOx interrupt is not triggered on the positive edge. (default)
When this bit = 1b, the corresponding GPIOx interrupt is triggered on the positive edge.

REG[0256h] GPIO Interrupt Status Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a						GPIO1 Negative Edge Interrupt Status	GPIO0 Negative Edge Interrupt Status
7	6	5	4	3	2	1	0
n/a						GPIO1 Positive Edge Interrupt Status	GPIO0 Positive Edge Interrupt Status

bits 9-8 GPIO[1:0] Negative Edge Interrupt Status
These bits indicate the status of the corresponding GPIOx Negative Edge Interrupt.
When this bit = 0b, a Negative Edge Interrupt has not occurred. (default)
When this bit = 1b, a Negative Edge Interrupt has occurred.

To clear this status bit, write a 1b to this bit.

bits 1-0 GPIO[1:0] Positive Edge Interrupt Status
These bits indicate the status of the corresponding GPIOx Positive Edge Interrupt.
When this bit = 0b, a Positive Edge Interrupt has not occurred. (default)
When this bit = 1b, a Positive Edge Interrupt has occurred.

To clear this status bit, write a 1b to this bit.

10.3.12 Command RAM Controller Registers

REG[0290h] Command RAM Controller Configuration Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a							Command RAM Access Read/Write Select

bit 0 Command RAM Access Read/Write Select
This bit selects whether the Command RAM is read from or written to when the Host accesses the Command RAM Access Port, REG[0294h].
When this bit = 0b, a read access is selected.
When this bit = 1b, a write access is selected.

REG[0292h] Command RAM Controller Address Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a				Command RAM Address Pointer bits 11-8			
7	6	5	4	3	2	1	0
Command RAM Address Pointer bits 7-0							

bits 11-0 Command RAM Address Pointer bits [11:0]
These bits specify the byte address in the Command RAM where data is read from or written to for each access to the Command RAM Access Port, REG[0294h]. After every access to REG[0294h], this register is auto incremented by +2.

REG[0294h] Command RAM Controller Access Port Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
Command RAM Access Port bits 15-8							
7	6	5	4	3	2	1	0
Command RAM Access Port bits 7-0							

bits 15-0 Command RAM Access Port bits [15:0]
These bits are the access port for the Command RAM.
For read accesses (REG[0290h] bit 0 = 0b), data is retrieved from the Command RAM address specified by REG[0292h] and can be read from these bits on the next read access to this register.
For write accesses (REG[0290h] bit 0 = 1b), these bits store the data that is written to the Command RAM address specified by REG[0292h].

10.3.13 Command Sequencer Controller Registers

REG[02A0h] Command Sequencer Controller Index Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
n/a		Command Sequencer Index Select bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 Command Sequencer Index Select bits [5:0]
These bits select the index for the Command Sequencer Data Port, REG[02A2h].

REG[02A2h] Command Sequencer Controller Data Port Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
Command Sequencer Data Port bits 15-8							
Command Sequencer Data Port bits 7-0							
7	6	5	4	3	2	1	0

bits 15-0 Command Sequencer Data Port bits [15:0]
These bits are the Command Sequencer Data Port where each Index data has the following bit configuration:
bits 15-13 are the Command Parameter Number
bits 9-0 are the Command RAM Address Pointer

10.3.14 Display Engine: Display Timing Configuration

REG[0300h] Frame Data Length Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a			Frame Data Length bits 12-8				
7	6	5	4	3	2	1	0
Frame Data Length bits 7-0							

bits 12-0 Frame Data Length bits [12:0]
These bits specify the frame data length, in lines.
Frame data length = REG[0300h] bits 12-0

REG[0302h] Frame Sync Length Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Frame Sync Length bits 7-0							

bits 7-0 Frame Sync Length bits [7:0]
These bits specify the frame sync length, in lines.
Frame sync length = (REG[0302h] bits 7-0) + 1

REG[0304h] Frame Begin/End Length Register
Default = 0104h Read/Write

15	14	13	12	11	10	9	8
Frame End Length bits 7-0							
7	6	5	4	3	2	1	0
Frame Begin Length bits 7-0							

bits 15-8 Frame End Length bits [7:0]
These bits specify the frame end length, in lines.
Frame end length = REG[0304h] bits 15-8

Note
These bits must be programmed such that the following formula is valid.
REG[0304h] bits 15-8 ≥ 1

bits 7-0 Frame Begin Length bits [7:0]
These bits specify the frame begin length, in lines.
Frame begin length = REG[0304h] bits 7-0

Note
These bits must be programmed according to the gate driver specification. For the Sharp LH1692, these bits must be set to 4h. For other generic Gate drivers, these bits must be set to 0h.

REG[0306h] Line Data Length Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a			Line Data Length bits 12-8				
7	6	5	4	3	2	1	0
Line Data Length bits 7-0							

bits 12-0 Line Data Length bits [12:0]
These bits specify the line data length, in pixels.
Line data length = REG[0306h] bits 12-0

Note
When 4 pixel output is selected (REG[030Ch] bit 11 = 0b), these bits must be set to a multiple of 4 pixels. When 8 pixel output is selected (REG[030Ch] bit 11 = 1b), these bits must be set to a multiple of 8 pixels.

REG[0308h] Line Sync Length Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Line Sync Length bits 7-0							

bits 7-0 Line Sync Length bits [7:0]
These bits specify the line sync length, in 4 pixel increments, and are offset by 4 or 8 pixels depending on the pixel output count

For 4 pixel output (REG[030Ch] bit 11 = 0b):
Line sync length = REG[0308h] bits 7-0 x 4 + 4 + 2)
For 8 pixel output (REG[030Ch] bit 11 = 1b):
Line sync length = REG[0308h] bits 7-0 x 4 + 8 + 2)

REG[030Ah] Line Begin/End Length Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
Line End Length bits 7-0							
7	6	5	4	3	2	1	0
Line Begin Length bits 7-0							

bits 15-8 Line End Length bits [7:0]
These bits specify the line end length, in 4 pixel increments.
Line end length = REG[030Ah] bits 15-8 x 4

bits 7-0 Line Begin Length bits [7:0]
These bits specify the line begin length, in 4 pixel increments.
Line begin length = REG[030Ah] bits 7-0 x 4

10.3.15 Display Engine: Driver Configurations

REG[030Ch] Source Driver Configuration Register
Default = 0064h Read/Write

Source Driver Chip Enable Start bits 3-0				Source Driver Pixel Output Count Select	Source Driver Chip Enable Reverse	Source Driver Output Reverse	Source Driver Shift Right
15	14	13	12	11	10	9	8
Source Driver Output Size Select bits 7-0							
7	6	5	4	3	2	1	0

bits 15-12 Source Driver Chip Enable Start bits [3:0]
These bits determine the number of the driver chip to start driving. The Source Driver Chip Enable Reverse bit (REG[030Ch] bit 10) can be used to reverse the chip enable sequence. For an example, see the following table.

Table 10-21: Example of Chip Enable Start + Chip Enable Reverse (ChipSize = 268, Line Size = 800)

REG[030Ch] bit 10	REG[030Ch] bits 15-12	Chip Enable Sequence
0b	0000b	Chip0 -> Chip1 -> Chip2
	0001b	Chip1 -> Chip2 -> Chip0
	0010b	Chip2 -> Chip0 -> Chip1
	0011b ~ 1111b	Reserved
1b	0000b	Chip0 -> Chip2 -> Chip1
	0001b	Chip1 -> Chip0 -> Chip2
	0010b	Chip2 -> Chip1-> Chip0
	0011b ~ 1111b	Reserved

bit 11 Source Driver Pixel Output Count Select
This bit selects the number of parallel pixels output per Source Driver clock.
When this bit = 0b, the source driver outputs 4 pixels per clock.
When this bit = 1b, the source driver outputs 8 pixels per clock.

bit 10 Source Driver Chip Enable Reverse
This bit configures the enable sequence for multiple chip selects. The number of chip selects is determined by the Line Data Length bits (REG[0306h] bits 12-0) and the Source Driver Output Size Select bits (REG[030Ch] bits 6-0). Using these bits with the Source Driver Chip Enable Start bit provides full configurability of the count down sequence.
When this bit = 0b, the source driver chip enable sequence is not reversed.
When this bit = 1b, the source driver chip enable sequence is reversed.

bit 9 Source Driver Output Reverse

This bit selects the parallel pixels output arrangement.

Table 10-22: Source Driver Output Reverse Function

REG[030Ch] bit 11	Pixels Arrangement in Little Endian	REG[030Ch] bit 9	Parallel Output to Source Driver
0	P3,P2,P1,P0	0	P3,P2,P1,P0
0	P3,P2,P1,P0	1	P0,P1,P2,P3
1	P7,P6,P5,P4,P3,P2,P1,P0	0	P7,P6,P5,P4,P3,P2,P1,P0
1	P7,P6,P5,P4,P3,P2,P1,P0	1	P0,P1,P2,P3,P4,P5,P6,P7

bit 8 Source Driver Shift Right

This bit determines how the source driver shifts the Serial to Parallel data.

When this bit = 0b, the serial to parallel data is shifted from Left to Right. The first data input is shifted from the last source driver output to the first source driver output (i.e. for 268 size, 268 -> 1). This means the first data accepted by the source driver will appear on the first line of the source driver.

When this bit = 1b, the serial to parallel data is shifted from Right to Left. The first data input is shifted from the first source driver output to the last source driver output (i.e. for 268 size, 1 -> 268). This means the first data accepted by the source driver will appear on the last line of the source driver.

bits 7-0 Source Driver Output Size Select bits [7:0]

These bits select the source driver output size per chip.

REG[030Ch] bits 7-0 = value in pixels x 4

Default = 0x64 (400d)

REG[030Eh] Gate Driver Configuration Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Source Driver SDOED Delay bits 4-0					Source Driver Double Data Rate Enable	Source Driver Swap Padding Pixels	Source Driver Early SDOE Assert Disable
7	6	5	4	3	2	1	0
Source Driver SDOEX Delay bits 4-0					n/a	Gate Driver Right/Left Select	Gate Driver Start Pulse Polarity

bits 15-11 Source Driver SDOED Delay bits [4:0]
These bits specify the SDOED (SDCE_L10 pin) delay from SDLE, in SDCLKs.

bit 10 Source Driver Double Data Rate Enable
This bit is used when the source driver pixel output count is set to 8 pixels.
When this bit = 0b, 8 pixels are output per SDCLK.
When this bit = 1b, the data rate is doubled and 4 pixels are output per SDCLK edge (positive and negative edges).

bit 9 Source Driver Swap Padding Pixels
This bit is used in combination with the Source Driver Shift Right bit (REG[030Ch] bit 8) and causes pixels padding whenever the Source Driver chip contains extra unused/non-display pixels.

Table 10-23: Source Driver Padding Pixels Position

REG[030Eh] bit 9	REG[030Ch] bit 8	Padding Data Location
0b	0b	Extra Pixels will be padded at the end of the Last Chip
0b	1b	Extra Pixels will be padded at the beginning of the First Chip
1b	0b	Extra Pixels will be padded at the beginning of the First Chip
1b	1b	Extra Pixels will be padded at the end of the Last Chip

bit 8 Source Driver Early SDOE Assert Disable
This bit determines whether SDOE is asserted 1 line early before SDLE in normal operation (for non-Micronix source drivers). This setting should be acceptable for Micronix source drivers also. However, if this method causes problems on Micronix source drivers, it can be disabled using this bit.
When this bit = 0b, Source Driver Early SDOE Assert is enabled.
When this bit = 1b, Source Driver Early SDOE Assert is disabled.

bits 7-3 Source Driver SDOEX Delay bits [4:0]
These bits specify the SDOEX (SDCE_L9 pin) delay from SDLE, in SDCLKs.

bit 1 Gate Driver Right/Left Select
This bit selects the gate driver GDRL pin output.
When this bit = 0b, the Gate Driver GDRL pin output is left.
When this bit = 1b, the Gate Driver GDRL pin output is right.

bit 0 Gate Driver Start Pulse Polarity
This bit controls the gate driver start pulse polarity.
When this bit = 0b, the polarity is negative.
When this bit = 1b, the polarity is positive.

10.3.16 Display Engine: Memory Region Configuration Registers

REG[0310h] Image Buffer Start Address Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Image Buffer Start Address bits 15-8							
7	6	5	4	3	2	1	0
Image Buffer Start Address bits 7-0							

REG[0312h] Image Buffer Start Address Register 1
Default = 0080h — Read/Write

15	14	13	12	11	10	9	8
n/a						Image Buffer Start Address bits 25-24	
7	6	5	4	3	2	1	0
Image Buffer Start Address bits 23-16							

REG[0312h] bits 9-0
REG[0310h] bits 15-0 Image Buffer Start Address bits [25:0]
These bits specify the Image Buffer start address in SDRAM byte address space.

REG[0314h] Update Buffer Start Address Register 0
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Update Buffer Start Address bits 15-8							
7	6	5	4	3	2	1	0
Update Buffer Start Address bits 7-0							

REG[0316h] Update Buffer Start Address Register 1
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
Update Buffer Start Address bits 31-24							
7	6	5	4	3	2	1	0
Update Buffer Start Address bits 23-16							

REG[0316h] bits 15-0
REG[0314h] bits 15-0 Update Buffer Start Address bits [31:0]
These bits specify the Update Buffer start address in SDRAM byte address space.

10.3.17 Display Engine: Component Control

REG[0320h] Temperature Device Select Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
n/a						Temperature Device Source Select	Temperature Auto Retrieval Disable

bit 1 Temperature Device Source Select
This bit selects between the I2C thermal sensor or the Dialog DA8590 IC for Temperature Sensing device. This bit must be set to 0b when the Dialog DA8590 IC is not present.
When this bit = 0b, the I2C thermal sensor is selected.
When this bit = 1b, the Dialog DA8590 IC is selected for power management.

bit 0 Temperature Auto Retrieval Disable
This bit determines whether the temperature is retrieved from the selected device (see bit 1) on every update frame operation.
When this bit = 0b, temperature retrieval is enabled. (default)
When this bit = 1b, temperature retrieval is disabled.

REG[0322h] Temperature Value Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Temperature Value bits 7-0							

bits 7-0 Temperature Value bits [7:0]
These bits store the temperature value which will be used for Waveform retrieval on the next display update operation. When Temperature Auto Retrieval is enabled (REG[0320h] bit 0 = 0b), these bits are automatically updated on every frame update operation.

REG[0324h] DWELL Time Configuration Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a							
7	6	5	4	3	2	1	0
Dwell Time Update Interval bits 7-0							

bits 7-0 Dwell Time Update Interval bits [7:0]
These bits specify the update intervals, in frames.

REG[0326h] Border Configuration Register 0
Default = 0000h — Read/Write

Saved - Next Border Value Status bits 7-0 (RO)							
15	14	13	12	11	10	9	8
Next Border Value Request bits 7-0							
7	6	5	4	3	2	1	0

bits 15-8 Saved - Next Border Value Status bits [7:0] (Read Only)
These bits indicate the saved Next Border Value which will be used for N-frame transfers.

bits 7-0 Next Border Value Control Request bits [7:0]
These bits specify the Next Border Value requested. Depending on the LUT index mode, the proper MSB bits will be selected for the LUT Index.

REG[0328h] Border Configuration Register 1
Default = 0000h — Read Only

Saved - Previous Border Value Status bits 1-0		n/a				Border Dwell Time bits 1-0	
15	14	13	12	11	10	9	8
Current Border Value bits 7-0							
7	6	5	4	3	2	1	0

bits 15-14 Saved - Previous Border Value Status bits [1:0] (Read Only)
These bits indicate the saved Current Border Value which will be used for N-frame transfers.

Note
If dwell time LUT Index Mode is selected, the Border Dwell time value is fixed to 3h (Max).

bits 9-8 Border Dwell Time bits [1:0] (Read Only)
These bits indicate the dwell time for Border updates.

bits 7-0 Saved - Current Border Value Control bits [7:0] (Read Only)
These bits indicate the saved Current Border Value which will be used for N-frame transfers.

REG[032Ah] Power Control Configuration Register

Default = 000Fh — Read/Write

15	14	13	12	11	10	9	8
n/a							Voltage Control Byte Force Frame Wait
7	6	5	4	3	2	1	0
Voltage Control Byte Wait Select bits 3-0				Voltage Control Byte 3 Enable	Voltage Control Byte 2 Enable	Voltage Control Byte 1 Enable	Voltage Control Byte 0 Enable

These bits are only active when the Waveform data format is version 1 - voltage control format. This bits correspond to the Version 1 waveform data which contains an additional 4 bytes at the beginning of each temperature compensated waveform data.

bit 8 — Voltage Control Byte Force Frame Wait
This bit forces the number of frames specified by REG[032Ah] bits 7-4 to be skipped before the next frame is displayed.

bits 7-4 — Voltage Control Byte Wait Select bits [3:0]
When the value of a voltage control byte changes, these bits specify the number of frames that are skipped before the next frame is displayed.

bit 3 — Voltage Control Byte 3 Enable
This bit controls Power Control programming.
When this bit = 0b, Voltage Control Byte 3 is disabled.
When this bit = 1b, Voltage Control Byte 3 is enabled.

bit 2 — Voltage Control Byte 2 Enable
This bit controls Power Control VCOMS programming.
When this bit = 0b, Voltage Control Byte 2 is disabled.
When this bit = 1b, Voltage Control Byte 2 is enabled.

bit 1 — Voltage Control Byte 1 Enable
This bit controls Power Control VEES/VCCS programming.
When this bit = 0b, Voltage Control Byte 1 is disabled.
When this bit = 1b, Voltage Control Byte 1 is enabled.

bit 0 — Voltage Control Byte 0 Enable
This bit controls Power Control VNEGS/VPOSS programming.
When this bit = 0b, Voltage Control Byte 0 is disabled.
When this bit = 1b, Voltage Control Byte 0 is enabled.

REG[032Ch] General Configuration Register
Default = 0000h — Read/Write

n/a					Area Coordinate End Size Select	Area Coordinate Rotation Select bits 1-0	
15	14	13	12	11	10	9	8
n/a		Display FIFO Threshold Select bits 1-0		n/a			
7	6	5	4	3	2	1	0

bit 10 — Area Coordinate End Size Select
This bit selects whether REG[0344h] ~ REG[0346h] define the X/Y end coordinates of the area update or the horizontal/vertical size of the area update relative to the X/Y start position (REG[0340h] ~ REG[0342h]).
When this bit = 0b, REG[0344h] ~ REG[0346h] define the X/Y end coordinates for the area update.
When this bit = 1b, REG[0344h] ~ REG[0346h] define the horizontal/vertical size for the area update.

bits 9-8 — Area Coordinate Rotation Select bits [1:0]
These bits select the rotation mode used to define the area update input coordinates (REG[0340h] ~ REG[0346h]).

Table 10-24 : Area Coordinate Rotation Selection

REG[032Ch] bits 9-8	Area Coordinate Rotation
00b	0°
01b	90°
10b	180°
11b	270°

bits 5-4 — Display FIFO Almost Empty Threshold Select bits [1:0]
These bits are used for debugging purposes only. These bits select the display FIFO condition that triggers a Display Pipe FIFO Underflow Interrupt which is indicated by REG[033Ah] bit 6.

Table 10-25 : Display FIFO Almost Empty Threshold Selection

REG[032Ch] bits 5-4	Display FIFO Threshold
00b (default)	Trigger REG[033Ah] bit 6 when FIFO is less than 1/2 full
01b	Trigger REG[033Ah] bit 6 when FIFO is less than 1/4 full
10b	Trigger REG[033Ah] bit 6 when FIFO is less than 3/4 full
11b	Trigger REG[033Ah] bit 6 when FIFO is not full

REG[032Eh] LUT Mask Register

Default = 0000h Read/Write

LUT 15 Mask 15	LUT 14 Mask 14	LUT 13 Mask 13	LUT 12 Mask 12	LUT 11 Mask 11	LUT 10 Mask 10	LUT 9 Mask 9	LUT 8 Mask 8
LUT 7 Mask 7	LUT 6 Mask 6	LUT 5 Mask 5	LUT 4 Mask 4	LUT 3 Mask 3	LUT 2 Mask 2	LUT 1 Mask 1	LUT 0 Mask 0

bits 15-0 LUT [15:0] Mask

These bits specify which LUTs (0-15) are included in the available status of the Masked LUT Status bit, REG[0338h] bit 6.

When this bit = 0b, the available status of LUTx is not included in REG[0338h] bit 6.

When this bit = 1b, the available status of LUTx is included in REG[0338h] bit 6.

10.3.18 Display Engine: Control/Trigger Registers

REG[0330h] Update Buffer Configuration Register
Default = 0000h — Read/Write

Display Engine Software Reset (WO)	n/a			Reserved			
15	14	13	12	11	10	9	8
LUT Auto Select Enable	Reserved	n/a		LUT Index Format Select bits 2-0			
7	6	5	4	3	2	1	0

bit 15 — Display Engine Software Reset (Write Only)
This bit performs a software reset of the display engine and resets the value of REG[0350h] to the default value.
Writing a 0b to this bit has no effect.
Writing a 1b to this bit initiates a software reset of the display engine.

bit 11-8 — Reserved
The default value for these bits is 0000b.

bit 7 — LUT Auto Select Enable
This bit determines whether the Look-Up Tables (LUTs) are manually selected using the Display Update LUT Select bit (REG[0334h] bits 7-4) or automatically selected from an available LUT. If Auto LUT Select is enabled, the Display Update LUT Select bits are ignored.
When this bit = 0b, LUT auto select is disabled.
When this bit = 1b, LUT auto select is enabled.

bit 6 — Reserved
The default value for this bit is 0b.

bits 2-0 — LUT Index Format Select bits [2:0]
These bits select the index format for the Look-Up Tables (LUTs).

Table 10-26 : LUT Index Format Selection

REG[0330h] bits 2-0	LUT Index Format
000b	P2N
001b	P2D
010b	P3N
011b	P3D
100b	P4N
101b	P4D
110b	P5N
111b	Reserved

REG[0332h] Update Buffer Pixel Set Value Register
Default = 0000h Read/Write

n/a							
15	14	13	12	11	10	9	8
Update Buffer Pixel Set Value bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Update Buffer Pixel Set Value bits [7:0]
These bits specify the pixel value for the Update Buffer Set Value Refresh operation, REG[0334h] bits 3-1 = 001b.

REG[0334h] Display Engine Control/Trigger Register
Default = 0000h Write/Read

3-Wire Chip Power Control Enable	Border Update Enable	Update Rectangle Mode bits 1-0		Display Update Waveform Mode bits 3-0			
15	14	13	12	11	10	9	8
Display Update LUT Select bits 3-0				Operation Mode bits 2-0			Operation Trigger (WO)
7	6	5	4	3	2	1	0

bit 15 3-Wire Chip Power Control Enable
This bit is only active when the Waveform data format is version 1 (voltage control format). This bit controls the 3-Wire Chip power control sequence used for programming the 3-Wire Chip (using Version 1 waveform data) on every display update trigger.
When this bit = 0b, the 3-Wire Chip power control sequence is disabled.
When this bit = 1b, the 3-Wire Chip power control sequence is enabled.

bit 14 Border Update Enable
This bit controls border updates.
When this bit = 0b, the border is not updated on the next display update (disabled).
When this bit = 1b, the border is updated on the next display update (enabled).

bits 13-12 Update Rectangle Mode bits [1:0]
These bits are used when the selected operation mode (see REG[0334h] bits 3-1) is set for Update Buffer Set Value Refresh, Update Buffer Image Buffer Refresh, Full Display Update, or Partial Display Update. These bits select the method used to define the update rectangle.

Table 10-27 : Update Rectangle Mode

REG[0334h] bits 13-12	Update Rectangle Mode
00b	Full Display Size Update
01b	Host X/Y Start/End positions are used (see REG[0348h] ~ REG[034Eh]
10b	X/Y Start/End positions are specified by REG[0340h] ~ REG[0346h]
11b	Reserved

bits 11-8 Display Update Waveform Mode Select bits [3:0]
These bits are only used for Operation Modes 3 and 4 (REG[0334h] bits 3-1 = 011b and 100b). These bits select the Waveform Mode for the display update.

bits 7-4 Display Update LUT Select bits [3:0]

These bits are only used for Operation Modes 3 and 4 (REG[0334h] bits 3-1 = 011b and 100b). These bits select the LUT (from LUT0 to LUT15) that is used for the display update. If the LUT Auto Select Enable bit is set (REG[0330h] bit 7 = 1b), these bits are ignored and the LUT is automatically selected.

bits 3-1 Operation Mode Select bits [2:0]

These bits select the operation mode that is triggered when the Operation Write Trigger bit is set, REG[0334h] bit 0 = 1b.

Table 10-28 : Operation Mode Selection

REG[0334h] bits 3-1	Operation Mode
000b	Waveform Header Read
001b	Update Buffer Set Value Refresh
010b	Update Buffer Image Buffer Refresh
011b	Full Display Update
100b	Partial Display Update
101b	Gate Driver Clear Operation
110b ~ 111b	Reserved

bit 0 Operation Write Trigger (Write Only)

This bit triggers a new operation as selected by REG[0334h] bits 3-1. If a new operation is triggered while the Operation Trigger Busy bit is set (REG[0338h] bit 0 = 1b), the operation trigger is ignored and an Operation Trigger Error Interrupt occurs (see REG[033Ah] ~ REG[033Ch] bit 8).

Writing a 0b to this bit has no effect.

Writing a 1b to this bit triggers a new operation.

10.3.19 Display Engine: Update Buffer Status Registers

REG[0336h] Lookup Table Status Register
Default = 0000h — Read Only

LUT15 Frame Update Busy	LUT14 Frame Update Busy	LUT13 Frame Update Busy	LUT12 Frame Update Busy	LUT11 Frame Update Busy	LUT10 Frame Update Busy	LUT9 Frame Update Busy	LUT8 Frame Update Busy
15	14	13	12	11	10	9	8
LUT7 Frame Update Busy	LUT6 Frame Update Busy	LUT5 Frame Update Busy	LUT4 Frame Update Busy	LUT3 Frame Update Busy	LUT2 Frame Update Busy	LUT1 Frame Update Busy	LUT0 Frame Update Busy
7	6	5	4	3	2	1	0

bits 15-0 LUT[15:0] Frame Update Busy (Read Only)
These bits indicate the status of the LUTx frame update. When a display update command for the corresponding LUT is issued, the LUT status will remain busy until all frames (N-Frames) have been transferred to the display.
When this bit = 0b, the corresponding LUT is not in use (idle).
When this bit = 1b, the corresponding LUT is in use (busy updating).

REG[0338h] Display Engine Busy Status Register
Default = 0000h — Read/Write

n/a			Serial Flash Checksum Error - N-Frame Compressed Data	Serial Flash Checksum Error - Region Pointer	Serial Flash Checksum Error - Mode Table	Serial Flash Checksum Error - Temperature Region	Serial Flash Checksum Error - Waveform Header
15	14	13	12	11	10	9	8
n/a	Masked LUT Available Status (RO)	LUT Available Status (RO)	Border Frame Busy (RO)	Display Frame Busy (RO)	Update Buffer Refresh Status (RO)	1 Frame Memory Access Busy (RO)	Operation Trigger Busy (RO)
7	6	5	4	3	2	1	0

bit 12 Serial Flash Checksum Error - N-Frame Compressed Data
This bit indicates whether a Serial Flash Checksum Error has occurred in the N-Frame Compressed Data.
When this bit = 0b, a serial flash checksum error has not occurred.
When this bit = 1b, a serial flash checksum error has occurred.

To clear this status bit, write a 1b to this bit.

bit 11 Serial Flash Checksum Error - Region Pointer
This bit indicates whether a Serial Flash Checksum Error has occurred in the Region Pointer.
When this bit = 0b, a serial flash checksum error has not occurred.
When this bit = 1b, a serial flash checksum error has occurred.

To clear this status bit, write a 1b to this bit.

bit 10 Serial Flash Checksum Error - Mode Table
This bit indicates whether a Serial Flash Checksum Error has occurred in the Mode Table.
When this bit = 0b, a serial flash checksum error has not occurred.
When this bit = 1b, a serial flash checksum error has occurred.

To clear this status bit, write a 1b to this bit.

bit 9	Serial Flash Checksum Error - Temperature Region This bit indicates whether a Serial Flash Checksum Error has occurred in the Temperature Region. When this bit = 0b, a serial flash checksum error has not occurred. When this bit = 1b, a serial flash checksum error has occurred. To clear this status bit, write a 1b to this bit.
bit 8	Serial Flash Checksum Error - Waveform Header This bit indicates whether a Serial Flash Checksum Error has occurred in the Waveform Header. When this bit = 0b, a serial flash checksum error has not occurred. When this bit = 1b, a serial flash checksum error has occurred. To clear this status bit, write a 1b to this bit.
bit 6	Masked LUT Available Status (Read Only) This bit indicates whether any of the LUTs (0-15) selected by the LUT Mask bits (REG[032Eh] bits 15-0) are currently available. When this bit = 0b, none of the selected LUTs are available. When this bit = 1b, at least one of the selected LUTs is available.
bit 5	LUT Available Status (Read Only) This bit indicates whether any LUTs are currently available. The number of available LUTs depends on the LUT Index Format, REG[0330h] bits 2-0. For P4D and P5N formats, only the first 4 LUTs are available. For all other formats, all 16 LUTs are available. When this bit = 0b, no LUTs are available. When this bit = 1b, at least one LUT is available.
bit 4	Border Frame Busy (Read Only) This bit indicates whether border frames are being output. When this bit = 0b, border frames are not being output (idle). When this bit = 1b, border frames are being output (busy).
bit 3	Display Frame Busy (Read Only) This bit indicates whether display frames are being output. When this bit = 0b, display frames are not being output (idle). When this bit = 1b, display frames are being output (busy).
bit 2	Update Buffer Refresh Status (Read Only) This bit indicates the status of update buffer refresh operations where the update buffer is written with new values. When this bit = 0b, the update buffer is not being refreshed. When this bit = 1b, the update buffer is being refreshed.
bit 1	1 Frame Memory Access Busy (Read Only) This bit indicates whether the memory is being accessed and will be set during any update buffer related memory access, including memory reads for display output. When this bit = 0b, memory is not being accessed (idle). When this bit = 1b, memory is being accessed (busy).

bit 0 Operation Trigger Busy (Read Only)

This bit indicates the status of the current operation (see (REG[0334h] bits 3-1) which is triggered by the Operation Write Trigger, REG[0334h] bit 0. While the selected operation is completed, this bit is automatically reset to 0b. If a new operation is triggered while this bit is set to 1b, the operation trigger is ignored and an Operation Trigger Error Interrupt occurs (see REG[033Ah] ~ REG[033Ch] bit 8).

When this bit = 0b, an operation is not being processed (idle).

When this bit = 1b, an operation is being processed (busy).

10.3.20 Display Engine: Interrupt Registers

REG[033Ah] Display Engine Interrupt Raw Status Register
Default = 0000h — Read/Write

15	14	13	12	11	10	9	8
n/a		Image Buffer Update Incomplete Interrupt Raw Status	Serial Flash Memory Checksum Error Interrupt Raw Status	Entry Count Mismatch Interrupt Raw Status	Temperature Out of Range Interrupt Raw Status	LUT Request Error Interrupt Raw Status	Operation Trigger Error Interrupt Raw Status
7	6	5	4	3	2	1	0
LUT Busy Conflict Detected Interrupt Raw Status	Display Pipe FIFO Underflow Interrupt Raw Status	All Frames Complete Interrupt Raw Status	Update Buffer Changed Interrupt Raw Status	One LUT N-Frame Display Complete Interrupt Raw Status	Display Output 1 Frame Complete Interrupt Raw Status	Update Buffer Refresh Done Interrupt Raw Status	Operation Trigger Done Interrupt Raw Status

bit 13 Image Buffer Update Incomplete Interrupt Raw Status

This bit indicates the raw status of the Image Buffer Update Incomplete Interrupt and is not masked by the Image Buffer Update Incomplete Interrupt Enable bit, REG[033Eh] bit 13. This interrupt occurs when the Display Engine begins reading data from the image buffer before the Host has completely written updated image data to the same buffer.
When this bit = 0b, a Image Buffer Update Incomplete Interrupt has not occurred.
When this bit = 1b, a Image Buffer Update Incomplete Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 13.

bit 12 Serial Flash Memory Checksum Error Interrupt Raw Status

This bit indicates the raw status of the Serial Flash Memory Checksum Error Interrupt and is not masked by the Serial Flash Memory Checksum Error Interrupt Enable bit, REG[033Eh] bit 12. To determine the cause of this interrupt, refer to the Serial Flash Memory Checksum Error Status bits, REG[0338h] bits 12-8.
When this bit = 0b, a Serial Flash Memory Checksum Error Interrupt has not occurred.
When this bit = 1b, a Serial Flash Memory Checksum Error Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 12.

bit 11 Entry Count Mismatch Interrupt Raw Status

This bit indicates the raw status of the Entry Count Mismatch Interrupt and is not masked by the Entry Count Mismatch Interrupt Enable bit, REG[033Eh] bit 11. This interrupt occurs when an unsupported entry count (see REG[0354h] bits 3-2) is selected for a Look-Up Table Index Format (see REG[0330h] bits 2-0). An entry count of 256 is only supported for index formats P2N, P2D, P3N, P3D, and P4N. An entry count of 1024 is only supported for index formats P4D and P5N. If a mismatch happens this bit is set and the update operation does not start.
When this bit = 0b, an Entry Count Mismatch Interrupt has not occurred.
When this bit = 1b, an Entry Count Mismatch Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 11.

bit 10 Temperature Out of Range Interrupt Raw Status

This bit indicates the raw status of the Temperature Out of Range Interrupt and is not masked by the Temperature Out of Range Interrupt Enable bit, REG[033Eh] bit 10. This interrupt occurs during a display frame request when the temperature is greater than, or less than, the temperature regions from the Waveform Table.

When this bit = 0b, a Temperature Out of Range Interrupt has not occurred.

When this bit = 1b, a Temperature Out of Range Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 10.

bit 9 LUT Request Error Interrupt Raw Status

This bit indicates the raw status of the LUT Request Error Interrupt and is not masked by the LUT Request Error Interrupt Enable bit, REG[033Eh] bit 9. This interrupt occurs an invalid LUT is requested by a triggered operation. An invalid LUT request happens when the requested LUT is currently in use (busy) or when auto LUT selection is enabled (REG[0330h] bit 7 = 1b) and no free LUTs are available. Note that for P5N and P4D index formats (see REG[0330h] bits 2-0), only the first four LUTs (0, 1, 2, and 3) are available.

When this bit = 0b, a LUT Request Error Interrupt has not occurred.

When this bit = 1b, a LUT Request Error Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 9.

bit 8 Operation Trigger Error Interrupt Raw Status

This bit indicates the raw status of the Operation Trigger Error Interrupt and is not masked by the Operation Trigger Error Interrupt Enable bit, REG[033Eh] bit 8. This interrupt occurs when a new operation is triggered (REG[0334h] bit 0 = 1b) while another operation is already being processed. If this happens, this bit is set and the operation trigger is ignored.

When this bit = 0b, an Operation Trigger Error Interrupt has not occurred.

When this bit = 1b, an Operation Trigger Error Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 8.

bit 7 LUT Busy Conflict Detected Interrupt Raw Status

This bit indicates the raw status of the LUT Busy Conflict Detected Interrupt and is not masked by the LUT Busy Conflict Detected Interrupt Enable bit, REG[033Eh] bit 7. This interrupt occurs during image buffer updates when a pixel update is required and the same pixel is currently being used for frame display (using another LUT).

When this bit = 0b, a LUT Busy Conflict Detected Interrupt has not occurred.

When this bit = 1b, a LUT Busy Conflict Detected Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 7.

bit 6 Display Pipe FIFO Underflow Interrupt Raw Status
This bit indicates the raw status of the Display Pipe FIFO Underflow Interrupt and is not masked by the Display Pipe FIFO Underflow Interrupt Enable bit, REG[033Eh] bit 6. This interrupt occurs when a new operation is triggered (REG[0334h] bit 0 = 1b) and a display pipe underflow error occurs.
When this bit = 0b, a Display Pipe FIFO Underflow Interrupt has not occurred.
When this bit = 1b, a Display Pipe FIFO Underflow Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 6.

bit 5 All Frames Completed Interrupt Raw Status
This bit indicates the raw status of the All Frames Completed Interrupt and is not masked by the All Frames Completed Interrupt Enable bit, REG[033Eh] bit 5. This interrupt occurs at the end of a display output operation when all frames are completed.
When this bit = 0b, an All Frames Completed Interrupt has not occurred.
When this bit = 1b, an All Frames Completed Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 5.

bit 4 Update Buffer Changed Interrupt Raw Status
This bit indicates the raw status of the Update Buffer Changed Interrupt and is not masked by the Update Buffer Changed Interrupt Enable bit, REG[033Eh] bit 4. This interrupt occurs on every write to the update buffer and may trigger multiple times even when the update buffer has not been completely updated.
When this bit = 0b, an Update Buffer Changed Interrupt has not occurred.
When this bit = 1b, an Update Buffer Changed Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 4.

bit 3 One LUT N-Frame Display Complete Interrupt Raw Status
This bit indicates the raw status of the One LUT N-Frame Display Complete Interrupt and is not masked by the One LUT N-Frame Display Complete Interrupt Enable bit, REG[033Eh] bit 3. This interrupt occurs when the N-Frames required for a LUT to update a pixel or pixels completes.
When this bit = 0b, a One LUT N-Frame Display Complete Interrupt has not occurred.
When this bit = 1b, a One LUT N-Frame Display Complete Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 3.

bit 2 Display Output 1 Frame Complete Interrupt Raw Status
This bit indicates the raw status of the Display Output 1 Frame Complete Interrupt and is not masked by the Display Output 1 Frame Complete Interrupt Enable bit, REG[033Eh] bit 2. This interrupt occurs when display output of 1 Frame to the output Gate and Source drivers completes.
When this bit = 0b, a Display Output 1 Frame Complete Interrupt has not occurred.
When this bit = 1b, a Display Output 1 Frame Complete Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 2.

bit 1 Update Buffer Refresh Done Interrupt Raw Status
This bit indicates the raw status of the Update Buffer Refresh Done Interrupt and is not masked by the Update Buffer Refresh Done Interrupt Enable bit, REG[033Eh] bit 1. This interrupt occurs when an update buffer refresh operation (Set Value, Refresh, Partial Update, or Full Update; see REG[0334h] bits 3-1) completes.
When this bit = 0b, an Update Buffer Refresh Done Interrupt has not occurred.
When this bit = 1b, an Update Buffer Refresh Done Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 1.

bit 0 Operation Trigger Done Interrupt Raw Status
This bit indicates the raw status of the Operation Trigger Done Interrupt and is not masked by the Operation Trigger Done Interrupt Enable bit, REG[033Eh] bit 0. This interrupt occurs when the operation triggered by REG[0334h] bit 0 is completes.
When this bit = 0b, an Operation Trigger Done Interrupt has not occurred.
When this bit = 1b, an Operation Trigger Done Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 0.

REG[033Ch] Display Engine Interrupt Masked Status Register
Default = 0000h Read/Write

15	14	13	12	11	10	9	8
n/a		Image Buffer Update Incomplete Interrupt Masked Status	Serial Flash Memory Checksum Error Interrupt Masked Status	Entry Count Mismatch Interrupt Masked Status	Temperature Out of Range Interrupt Masked Status	LUT Request Error Interrupt Masked Status	Operation Trigger Error Interrupt Masked Status
7	6	5	4	3	2	1	0
LUT Busy Conflict Detected Interrupt Masked Status	Display Pipe FIFO Underflow Interrupt Masked Status	All Frames Complete Interrupt Masked Status	Update Buffer Changed Interrupt Masked Status	One LUT N-Frame Display Complete Interrupt Masked Status	Display Output 1 Frame Complete Interrupt Masked Status	Update Buffer Refresh Done Interrupt Masked Status	Operation Trigger Done Interrupt Masked Status

bit 13 Image Buffer Update Incomplete Interrupt Masked Status
This bit indicates the masked status of the Image Buffer Update Incomplete Interrupt (see REG[033Eh] bit 13). This interrupt occurs when the Display Engine begins reading data from the image buffer before the Host has completely written updated image data to the same buffer.
When this bit = 0b, a Image Buffer Update Incomplete Interrupt has not occurred.
When this bit = 1b, a Image Buffer Update Incomplete Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 13.

bit 12 Serial Flash Memory Checksum Error Interrupt Masked Status
This bit indicates the masked status of the Serial Flash Memory Checksum Error Interrupt (see REG[033Eh] bit 12). To determine the cause of this interrupt, refer to the Serial Flash Memory Checksum Error Status bits, REG[0338h] bits 12-8.
When this bit = 0b, a Serial Flash Memory Checksum Error Interrupt has not occurred.
When this bit = 1b, a Serial Flash Memory Checksum Error Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 12.

bit 11 Entry Count Mismatch Interrupt Masked Status
This bit indicates the masked status of the Entry Count Mismatch Interrupt (see REG[033Eh] bit 11). This interrupt occurs when an unsupported entry count (see REG[0354h] bits 3-2) is selected for a Look-Up Table Index Format (see REG[0330h] bits 2-0). An entry count of 256 is only supported for index formats P2N, P2D, P3N, P3D, and P4N. An entry count of 1024 is only supported for index formats P4D and P5N. If a mismatch happens this bit is set and the update operation does not start.
When this bit = 0b, an Entry Count Mismatch Interrupt has not occurred.
When this bit = 1b, an Entry Count Mismatch Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 11.

bit 10 Temperature Out of Range Interrupt Masked Status
This bit indicates the masked status of the Temperature Out of Range Interrupt (see REG[033Eh] bit 10). This interrupt occurs during a display frame request when the temperature is greater than, or less than, the temperature regions from the Waveform Table.
When this bit = 0b, a Temperature Out of Range Interrupt has not occurred.
When this bit = 1b, a Temperature Out of Range Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 10.

bit 9 LUT Request Error Interrupt Masked Status
This bit indicates the masked status of the LUT Request Error Interrupt (see REG[033Eh] bit 9). This interrupt occurs an invalid LUT is requested by a triggered operation. An invalid LUT request happens when the requested LUT is currently in use (busy) or when auto LUT selection is enabled (REG[0330h] bit 7 = 1b) and no free LUTs are available. Note that for P5N and P4D index formats (see REG[0330h] bits 2-0), only the first four LUTs (0, 1, 2, and 3) are available.
When this bit = 0b, a LUT Request Error Interrupt has not occurred.
When this bit = 1b, a LUT Request Error Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 9.

bit 8 Operation Trigger Error Interrupt Masked Status
This bit indicates the masked status of the Operation Trigger Error Interrupt (see REG[033Eh] bit 8). This interrupt occurs when a new operation is triggered (REG[0334h] bit 0 = 1b) while another operation is already being processed. If this happens, this bit is set and the operation trigger is ignored.
When this bit = 0b, an Operation Trigger Error Interrupt has not occurred.
When this bit = 1b, an Operation Trigger Error Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 8.

bit 7 LUT Busy Conflict Detected Interrupt Masked Status
This bit indicates the masked status of the LUT Busy Conflict Detected Interrupt (see REG[033Eh] bit 7). This interrupt occurs during image buffer updates when a pixel update is required and the same pixel is currently being used for frame display (using another LUT).
When this bit = 0b, a LUT Busy Conflict Detected Interrupt has not occurred.
When this bit = 1b, a LUT Busy Conflict Detected Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 7.

bit 6 Display Pipe FIFO Underflow Interrupt Masked Status
This bit indicates the masked status of the Display Pipe FIFO Underflow Interrupt (see REG[033Eh] bit6). This interrupt occurs when a new operation is triggered (REG[0334h] bit 0 = 1b) and a display pipe underflow error occurs.
When this bit = 0b, a Display Pipe FIFO Underflow Interrupt has not occurred.
When this bit = 1b, a Display Pipe FIFO Underflow Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 6.

bit 5 All Frames Completed Interrupt Masked Status
This bit indicates the masked status of the All Frames Completed Interrupt (see REG[033Eh] bit 5). This interrupt occurs at the end of a display output operation when all frames are completed.
When this bit = 0b, an All Frames Completed Interrupt has not occurred.
When this bit = 1b, an All Frames Completed Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 5.

bit 4 Update Buffer Changed Interrupt Masked Status
This bit indicates the masked status of the Update Buffer Changed Interrupt (see REG[033Eh] bit 4). This interrupt occurs on every write to the update buffer and may trigger multiple times even when the update buffer has not been completely updated.
When this bit = 0b, an Update Buffer Changed Interrupt has not occurred.
When this bit = 1b, an Update Buffer Changed Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 4.

bit 3 One LUT N-Frame Display Complete Interrupt Masked Status
This bit indicates the masked status of the One LUT N-Frame Display Complete Interrupt (see REG[033Eh] bit 3). This interrupt occurs when the N-Frames required for a LUT to update a pixel or pixels completes.
When this bit = 0b, a One LUT N-Frame Display Complete Interrupt has not occurred.
When this bit = 1b, a One LUT N-Frame Display Complete Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 3.

bit 2 Display Output 1 Frame Complete Interrupt Masked Status
This bit indicates the masked status of the Display Output 1 Frame Complete Interrupt (see REG[033Eh] bit 2). This interrupt occurs when display output of 1 Frame to the output Gate and Source drivers completes.
When this bit = 0b, a Display Output 1 Frame Complete Interrupt has not occurred.
When this bit = 1b, a Display Output 1 Frame Complete Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 2.

bit 1 Update Buffer Refresh Done Interrupt Masked Status
This bit indicates the masked status of the Update Buffer Refresh Done Interrupt (see REG[033Eh] bit 1). This interrupt occurs when an update buffer refresh operation (Set Value, Refresh, Partial Update, or Full Update; see REG[0334h] bits 3-1) completes.
When this bit = 0b, an Update Buffer Refresh Done Interrupt has not occurred.
When this bit = 1b, an Update Buffer Refresh Done Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 1.

bit 0 Operation Trigger Done Interrupt Masked Status
This bit indicates the masked status of the Operation Trigger Done Interrupt (see REG[033Eh] bit 0). This interrupt occurs when the operation triggered by REG[0334h] bit 0 is completes.
When this bit = 0b, an Operation Trigger Done Interrupt has not occurred.
When this bit = 1b, an Operation Trigger Done Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 0.

REG[033Eh] Display Engine Interrupt Enable Register
Default = 0000h Read Only

15	14	13	12	11	10	9	8
n/a		Image Buffer Update Incomplete Interrupt Enable	Serial Flash Memory Checksum Error Interrupt Enable	Entry Count Mismatch Interrupt Enable	Temperature Out of Range Interrupt Enable	LUT Request Error Interrupt Enable	Operation Trigger Error Interrupt Enable
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LUT Busy Conflict Detected Interrupt Enable	Display Pipe FIFO Underflow Interrupt Enable	All Frames Complete Interrupt Enable	Update Buffer Changed Interrupt Enable	One LUT N-Frame Display Complete Interrupt Enable	Display Output 1 Frame Complete Interrupt Enable	Update Buffer Refresh Done Interrupt Enable	Operation Trigger Done Interrupt Enable

bit 13 Image Buffer Update Incomplete Interrupt Enable
This bit controls whether the Image Buffer Update Incomplete Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 13 (unmasked) or REG[033Ch] bit 13 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 12 Serial Flash Memory Checksum Error Interrupt Enable
This bit controls whether the Serial Flash Memory Checksum Error Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 12 (unmasked) or REG[033Ch] bit 12 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 11 Entry Count Mismatch Interrupt Enable
This bit controls whether the Entry Count Mismatch Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 11 (unmasked) or REG[033Ch] bit 11 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 10 Temperature Out of Range Interrupt Enable
This bit controls whether the Temperature Out of Range Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 10 (unmasked) or REG[033Ch] bit 10 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 9 LUT Request Error Interrupt Enable
This bit controls whether the LUT Request Error Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 9 (unmasked) or REG[033Ch] bit 9 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 8 Operation Trigger Error Interrupt Enable
This bit controls whether the Operation Trigger Error Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 8 (unmasked) or REG[033Ch] bit 8 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 7 LUT Busy Conflict Detected Interrupt Enable
This bit controls whether the LUT Busy Conflict Detected Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 7 (unmasked) or REG[033Ch] bit 7 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 6 Display Pipe FIFO Underflow Interrupt Enable
This bit controls whether the Display Pipe FIFO Underflow Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 6 (unmasked) or REG[033Ch] bit 6 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 5 All Frames Complete Interrupt Enable
This bit controls whether the All Frames Complete Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 5 (unmasked) or REG[033Ch] bit 5 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 4 Update Buffer Changed Interrupt Enable
This bit controls whether the Update Buffer Changed Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 4 (unmasked) or REG[033Ch] bit 4 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 3 One LUT N-Frame Display Complete Interrupt Enable
This bit controls whether the One LUT N-Frame Display Complete Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 3 (unmasked) or REG[033Ch] bit 3 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 2 Display Output 1 Frame Complete Interrupt Enable
This bit controls whether the Display Output 1 Frame Complete Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 2 (unmasked) or REG[033Ch] bit 2 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 1 Update Buffer Refresh Done Interrupt Enable
This bit controls whether the Update Buffer Refresh Done Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 1 (unmasked) or REG[033Ch] bit 1 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

bit 0 Operation Trigger Done Interrupt Enable
This bit controls whether the Operation Trigger Done Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 0 (unmasked) or REG[033Ch] bit 0 (masked).
When this bit = 0b, the interrupt is disabled.
When this bit = 1b, the interrupt is enabled.

10.3.21 Display Engine: Partial Update Configuration Register

REG[0340h] Area Update Pixel Rectangular X-Start Register
Default = 0000h Read/Write

Area Update Pixel Rectangular X-Start Position bits 11-8							
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular X-Start Position bits 7-0							
7	6	5	4	3	2	0	0

bits 15-0 Area Update Pixel Rectangular X-Start Position bits [15:0]
When the Update Rectangle Mode bits are set for user configured X/Y Start/End (REG[0334h] bits 13-12 = 10b), these bits specify the X start position of the rectangular area to be updated, relative to the top left of the rotated image.

REG[0342h] Area Update Pixel Rectangular Y-Start Register
Default = 0000h Read/Write

Area Update Pixel Rectangular Y-Start Position bits 15-8							
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular Y-Start Position bits 7-0							
7	6	5	4	3	2	0	0

bits 15-0 Area Update Pixel Rectangular Y-Start Position bits [15:0]
When the Update Rectangle Mode bits are set for user configured X/Y Start/End (REG[0334h] bits 13-12 = 10b), these bits specify the Y start position of the rectangular area to be updated, relative to the top left of the rotated image.

REG[0344h] Area Update Pixel Rectangular X-End / Horizontal Size Register
Default = 0000h Read/Write

Area Update Pixel Rectangular X-End Position / Horizontal Size bits 15-8							
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular X-End Position / Horizontal Size bits 7-0							
7	6	5	4	3	2	0	0

bits 15-0 Area Update Pixel Rectangular X-End Position / Horizontal Size bits [15:0]
When the Update Rectangle Mode bits are set for user configured X/Y Start/End (REG[0334h] bits 13-12 = 10b), these bits specify either the X end position or the horizontal size (see REG[032Ch] bit 10) of the rectangular area to be updated, relative to the top left of the rotated image.

REG[0346h] Area Update Pixel Rectangular Y-End / Vertical Size Register
Default = 0000h Read/Write

Area Update Pixel Rectangular Y-End Position / Vertical Size bits 15-8							
15	14	13	12	11	10	9	8
Area Update Pixel Rectangular Y-End Position / Vertical Size bits 7-0							
7	6	5	4	3	2	0	0

bits 15-0 Area Update Pixel Rectangular Y-End Position / Vertical Size bits [15:0]
When the Update Rectangle Mode bits are set for user configured X/Y Start/End (REG[0334h] bits 13-12 = 10b), these bits specify either the Y end position or the vertical size (see REG[032Ch] bit 10) of the rectangular area to be updated, relative to the top left of the rotated image.

REG[0348h] Host Pixel Rectangular X-Start Register
Default = 0000h Read Only

Host Pixel Rectangular X-Start Position bits 15-8							
15	14	13	12	11	10	9	8
Host Pixel Rectangular X-Start Position bits 7-0							
7	6	5	4	3	2	0	0

bits 15-0 Host Pixel Rectangular X-Start Position bits [15:0] (Read Only)
When the Update Rectangle Mode bits are set for copy Host X/Y Start/End (REG[0334h] bits 13-12 = 01b), these bits indicate the X start position of the rectangular area that is updated.

REG[034Ah] Host Pixel Rectangular Y-Start Register
Default = 0000h Read Only

Host Pixel Rectangular Y-Start Position bits 15-8							
15	14	13	12	11	10	9	8
Host Pixel Rectangular Y-Start Position bits 7-0							
7	6	5	4	3	2	0	0

bits 15-0 Host Pixel Rectangular Y-Start Position bits [15:0] (Read Only)
When the Update Rectangle Mode bits are set for copy Host X/Y Start/End (REG[0334h] bits 13-12 = 01b), these bits indicate the Y start position of the rectangular area that is updated.

REG[034Ch] Host Pixel Rectangular X-End Register
Default = 0000h Read Only

Host Pixel Rectangular X-End Position bits 15-8							
15	14	13	12	11	10	9	8
Host Pixel Rectangular X-End Position bits 7-0							
7	6	5	4	3	2	0	0

bits 15-0 Host Pixel Rectangular X-End Position bits [15:0] (Read Only)
When the Update Rectangle Mode bits are set for copy Host X/Y Start/End (REG[0334h] bits 13-12 = 01b), these bits indicate the X end position of the rectangular area that is updated.

REG[034Eh] Host Pixel Rectangular Y-End Register
Default = 0000h Read Only

Host Pixel Rectangular Y-End Position bits 15-8							
15	14	13	12	11	10	9	8
Host Pixel Rectangular Y-End Position bits 7-0							
7	6	5	4	3	2	0	0

bits 15-0 Host Pixel Rectangular Y-End Position bits [15:0] (Read Only)
When the Update Rectangle Mode bits are set for copy Host X/Y Start/End (REG[0334h] bits 13-12 = 01b), these bits indicate the Y end position of the rectangular area that is updated.

10.3.22 Display Engine: Serial Flash Waveform Registers

REG[0350h] Waveform Header Serial Flash Address Register 0							
Default = 0000h							Read/Write
Waveform Header Serial Flash Address bits 15-8							
15	14	13	12	11	10	9	8
Waveform Header Serial Flash Address bits 7-0							
7	6	5	4	3	2	1	0

REG[0352h] Waveform Header Serial Flash Address Register 0							
Default = 0000h							Read/Write
n/a							
15	14	13	12	11	10	9	8
Waveform Header Serial Flash Address bits 23-16							
7	6	5	4	3	2	1	0

REG[0352h] bits 7-0
REG[0350h] bits 15-0 Waveform Header Serial Flash Address bits [23:0]
These bits store the Waveform Header start address in the Flash Memory.

REG[0354h] through REG[035Eh] are Reserved

These registers are Reserved and should not be written.

Chapter 11 Display Configurations

11.1 Display Memory Area Setup

The S1D13521 controller supports a single display region with destructive partial region writes only. A predefined memory start region can be defined using the Host commands (see Section 9.4, “Command List” on page 51). The memory start region is referenced as the Image Buffer Start Address position in the memory.

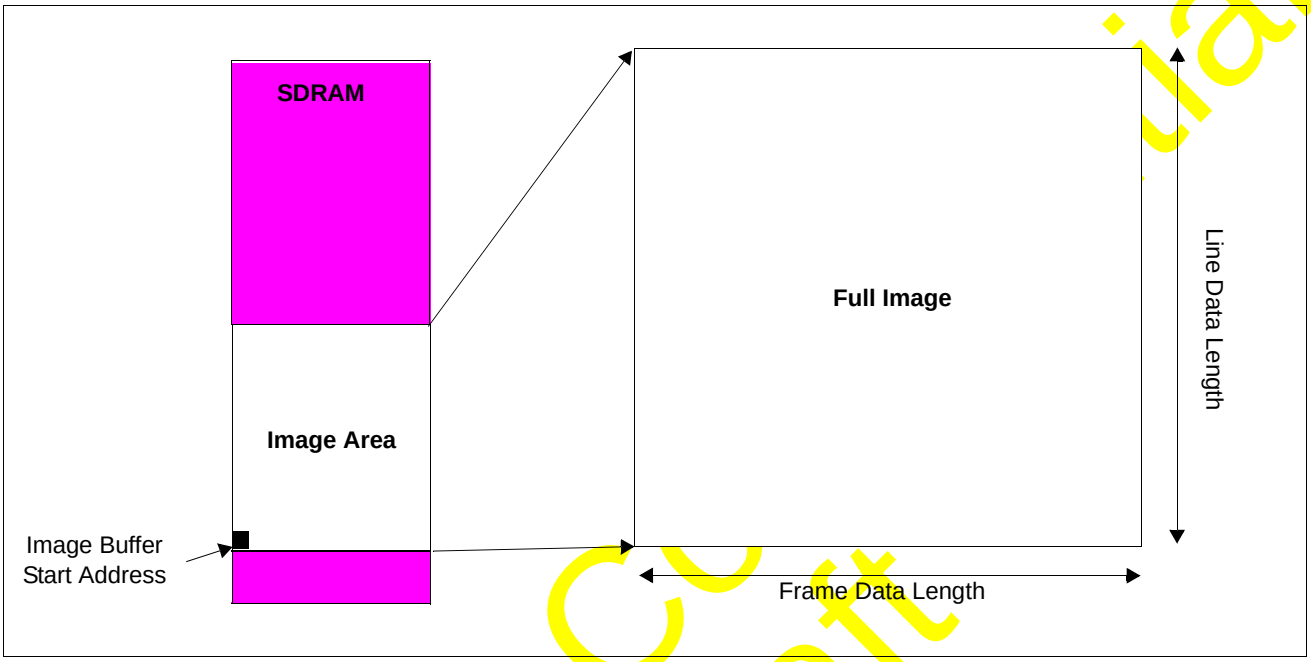


Figure 11-1: Full Image Area Setup

For any partial write using the predefined area (XStart, YStart, Width, and Height parameters), the S1D13521 automatically calculates the start memory address position.

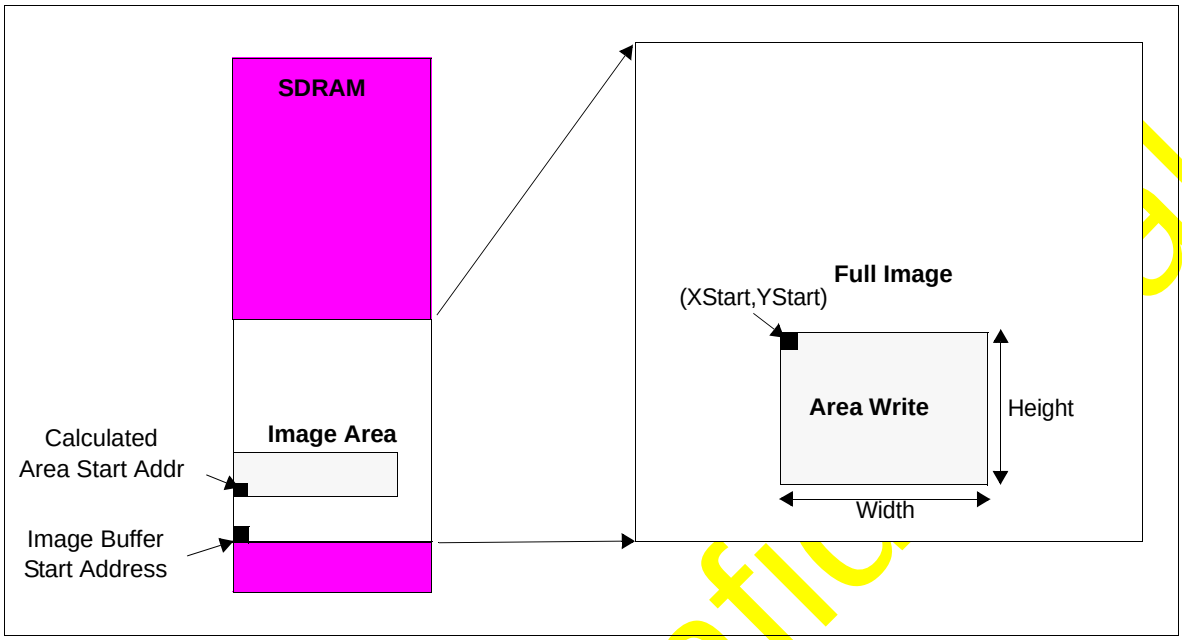


Figure 11-2: Host Memory Area Setup

11.2 Display Memory Bpp Mode

This S1D13521 stores every pixel in unpacked 1 byte format. The following figure shows how data is formatted using this single byte storage.

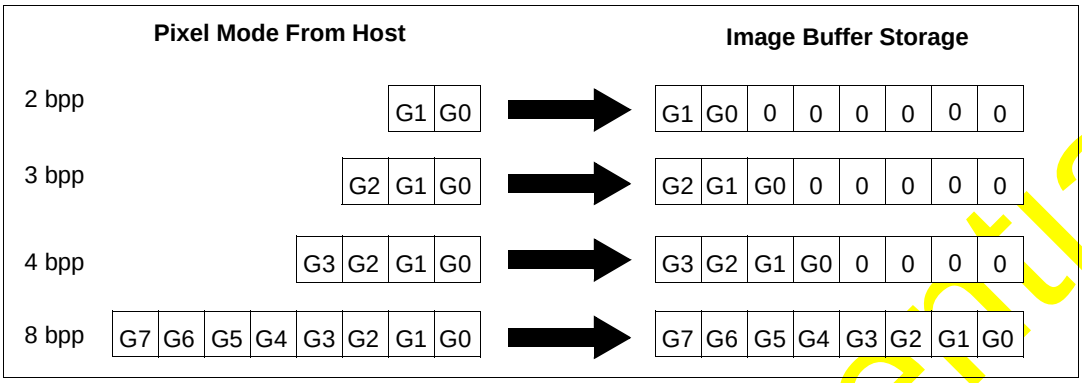


Figure 11-3: Bpp Mode Memory Storage

Note

For 8 bpp mode, the LUT index format (REG[0330h] bits 2-0) determines which MSB bits are used.

5 bpp – (G7-G3)
4 bpp – (G7-G4)
3 bpp – (G7-G5)
2 bpp – (G7-G6)

11.3 Host Interface Pixel Data Transfer Format

Data transfer from the Host interface always uses packed pixel format. Packed pixels are always arranged using the little endian arrangement. The following figure shows the host transfer data format of four pixel mode.

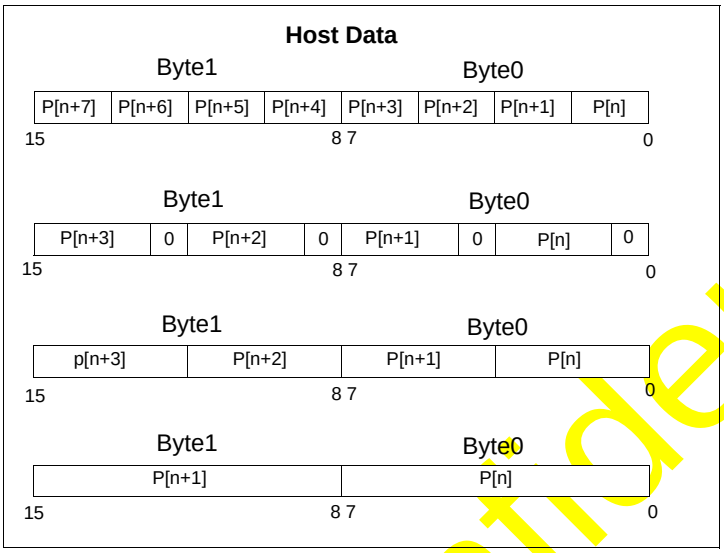


Figure 11-4: Host Interface Pixel Data Transfer Format

The packed pixel format requires certain limitations to be observed for all host image data transfers. The following size limitations must be observed for each bpp mode.

Table 11-1: Host Interface Pixel Data Transfer Limitations

Bpp Mode	Width limitation	Height limitation
2 bpp	Must be multiple of 8 pixels	Minimum of 1 Line
3 bpp	Must be multiple of 4 pixels	Minimum of 1 Line
4 bpp	Must be multiple of 4 pixels	Minimum of 1 Line
5/8 bpp	Must be multiple of 2 pixels	Minimum of 1 Line

11.4 Rotation Support

11.4.1 Rotation Introduction

Display panels are typically oriented in Landscape mode, where the Horizontal Size is larger than the Vertical Size. In this case, the display refresh occurs from Left to right and top to bottom.

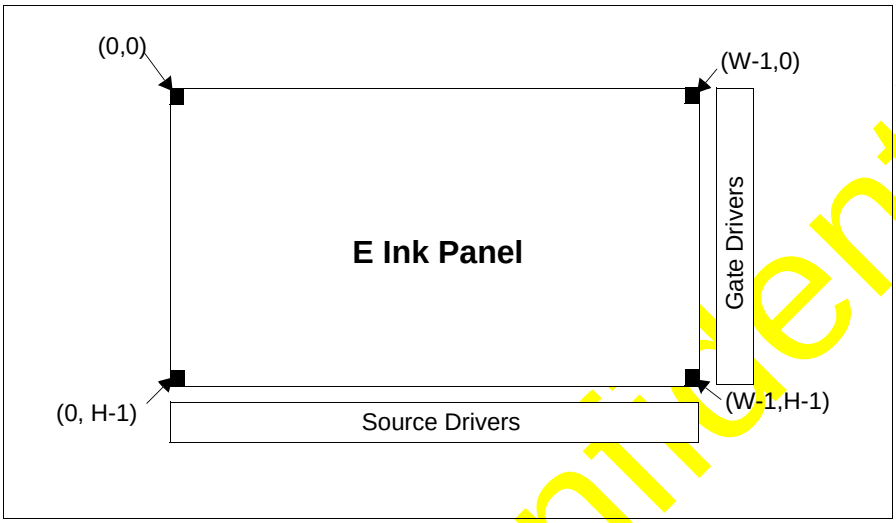


Figure 11-5: Landscape (0 Degrees) Display

The S1D13521 supports rotation modes that allow 90°, 180°, and 270° rotation in a counter-clockwise direction. The rotation is done in hardware and is transparent to the user for all display buffer writes.

The actual address translation is performed during the Host Write and the image data is stored in memory in the rotated orientation.

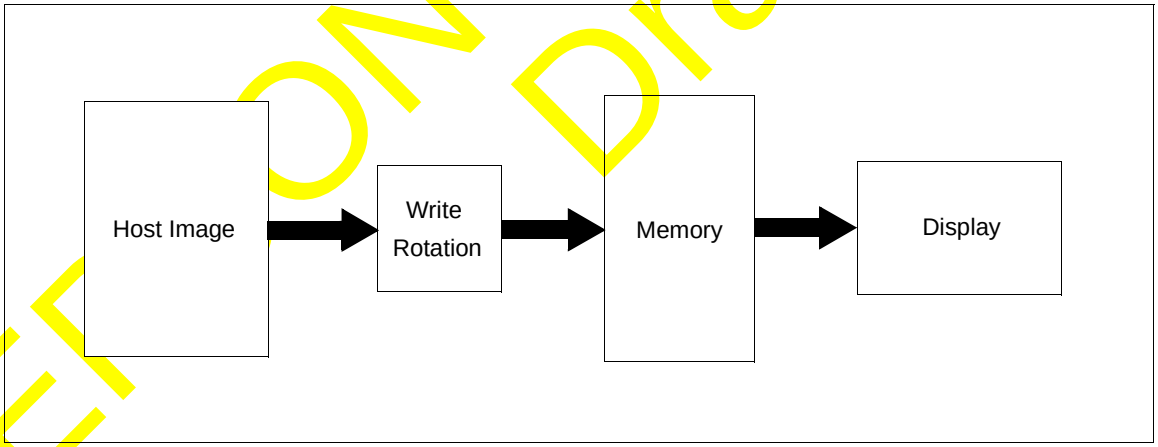


Figure 11-6: Write Rotation Flow in Hardware

Note
Memory Readback data does not support reverse-rotation.

11.4.2 90° Rotation

The following figure shows how the programmer sees a 600x800 portrait image and how the image is being displayed. The application image is written to the S1D13521 in the following sense: A–B–C–D. The display is refreshed in the following sense: B-D-A-C.

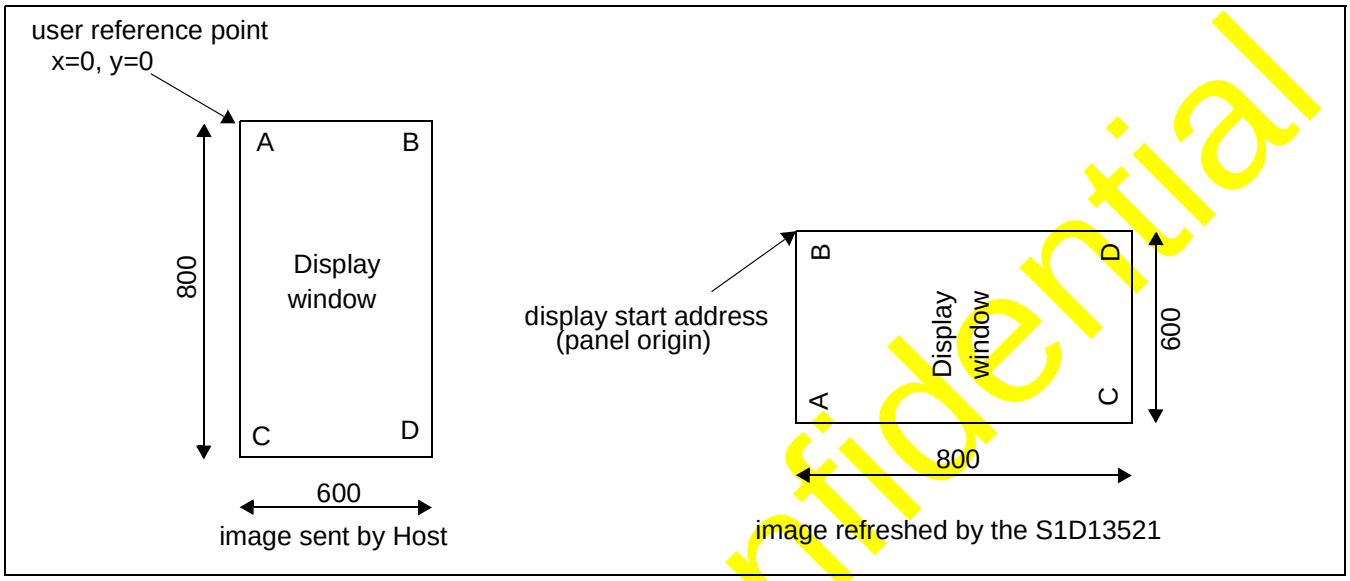


Figure 11-7: Relationship Between the Screen Image and the Image Refreshed in 90° Rotation

Programming

There are no special programming requirements other than enabling the rotation (see REG[0140h] bits 9-8). The start address and line offset are automatically calculated by the hardware.

11.4.3 180° Rotation

The following figure shows how the programmer sees a 800x600 landscape image and how the image is being displayed. The application image is written to the S1D13521 in the following sense: A–B–C–D. The display is refreshed in the following sense: D-C-B-A.

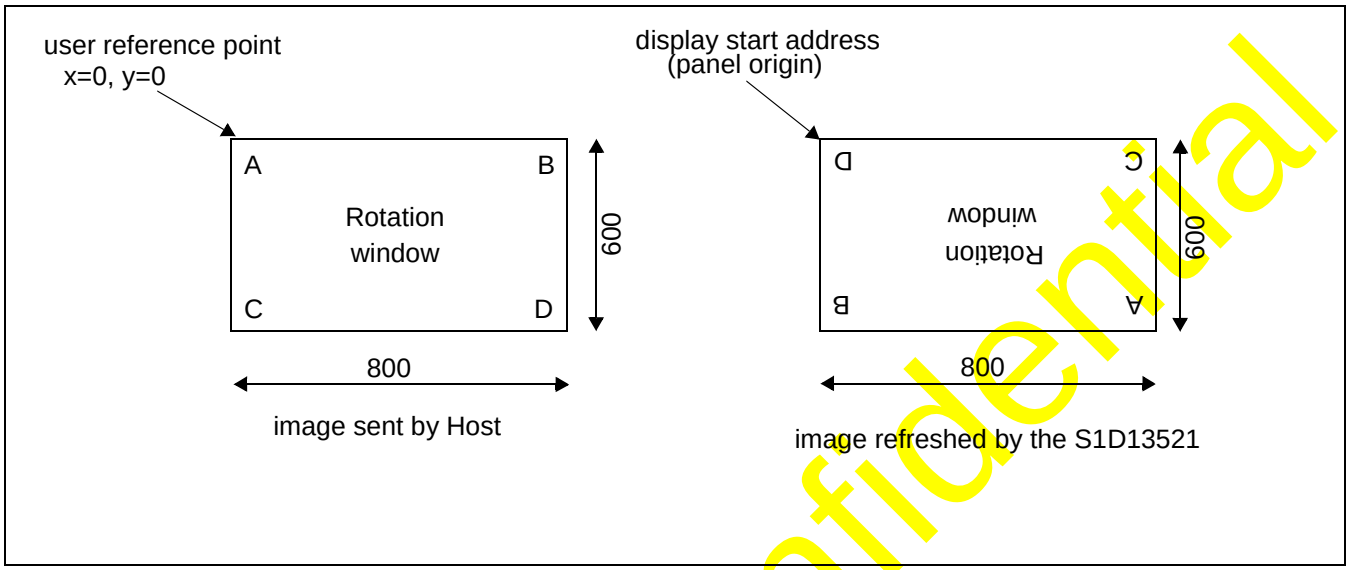


Figure 11-8: Relationship Between the Screen Image and the Image Refreshed in 180° Rotation

Programming

There are no special programming requirements other than enabling the rotation (see REG[0140h] bits 9-8). The start address and line offset are automatically calculated by the hardware.

11.4.4 270° Rotation

The following figure shows how the programmer sees a 600x800 portrait image and how the image is being displayed. The application image is written to the S1D13521 in the following sense: A–B–C–D. The display is refreshed in the following sense: C-A-D-B.

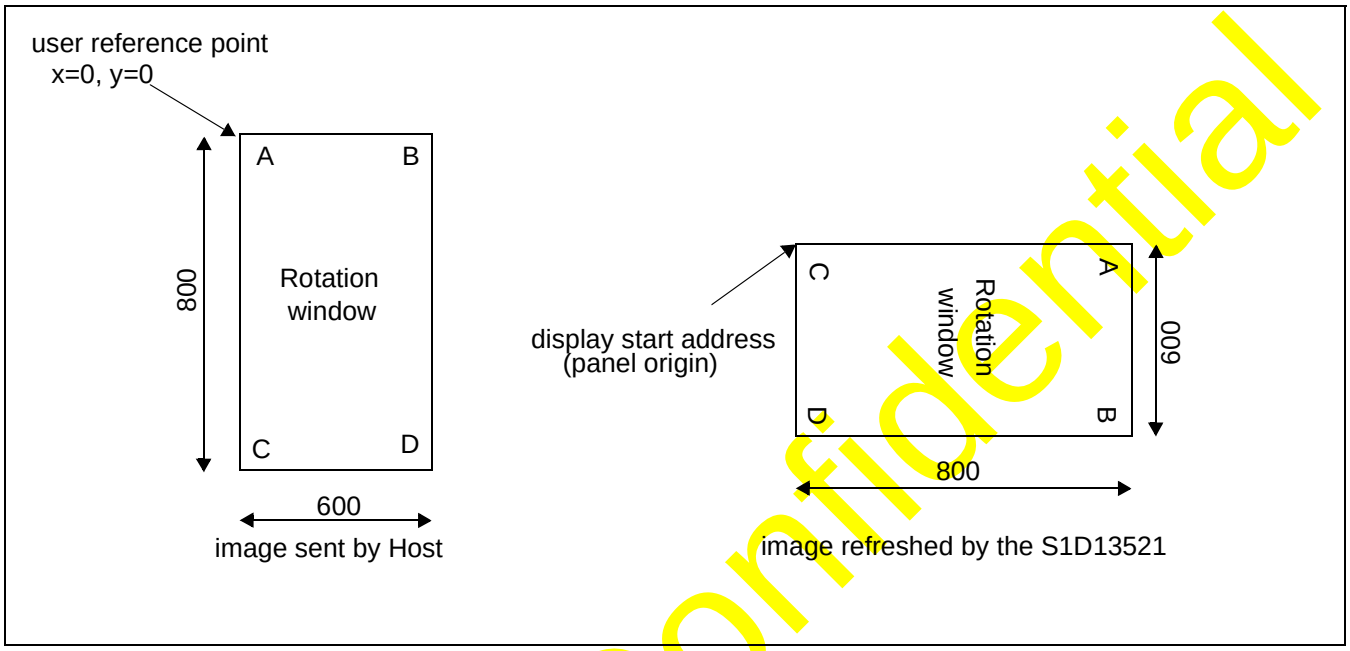


Figure 11-9: Relationship Between the Screen Image and the Image Refreshed in 270° Rotation

Programming

There are no special programming requirements other than enabling the rotation (see REG[0140h] bits 9-8). The start address and line offset are automatically calculated by the hardware.

11.5 Window Area Position / Rotation

For a Windowed Area write operation when rotation is enabled, the X-Start, Y-Start, Width and Height settings must be specified relative to **the user's own reference point**.

11.5.1 90° Rotation

The following figure shows how the Windowed Area is rotated on the displayed image. The application Window Area is written to the S1D13521 in the following sense: a–b–c–d.

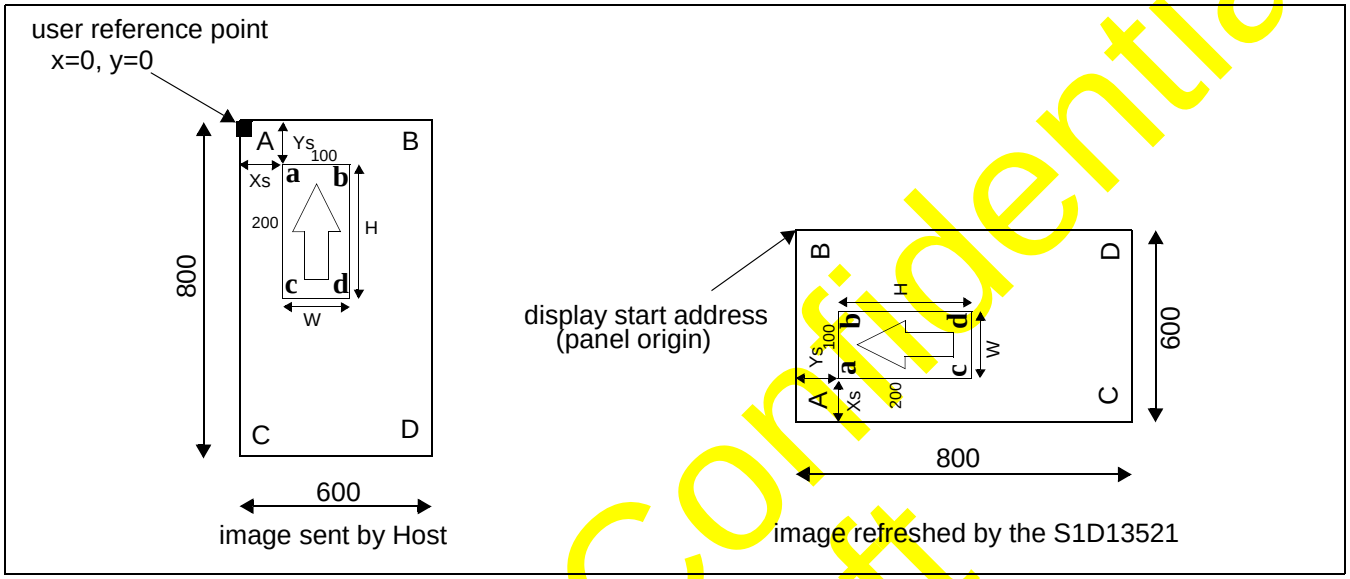


Figure 11-10: Relationship Between the Screen Window Area and the Image Refreshed in 90° Rotation

Programming

There are no special programming requirements other than enabling the rotation (see REG[0140h] bits 9-8). The start address and line offset are automatically calculated by the hardware.

11.5.2 180° Rotation

The following figure shows how the Windowed Area is rotated on the displayed image. The application Window Area is written to the S1D13521 in the following sense: a–b–c–d.

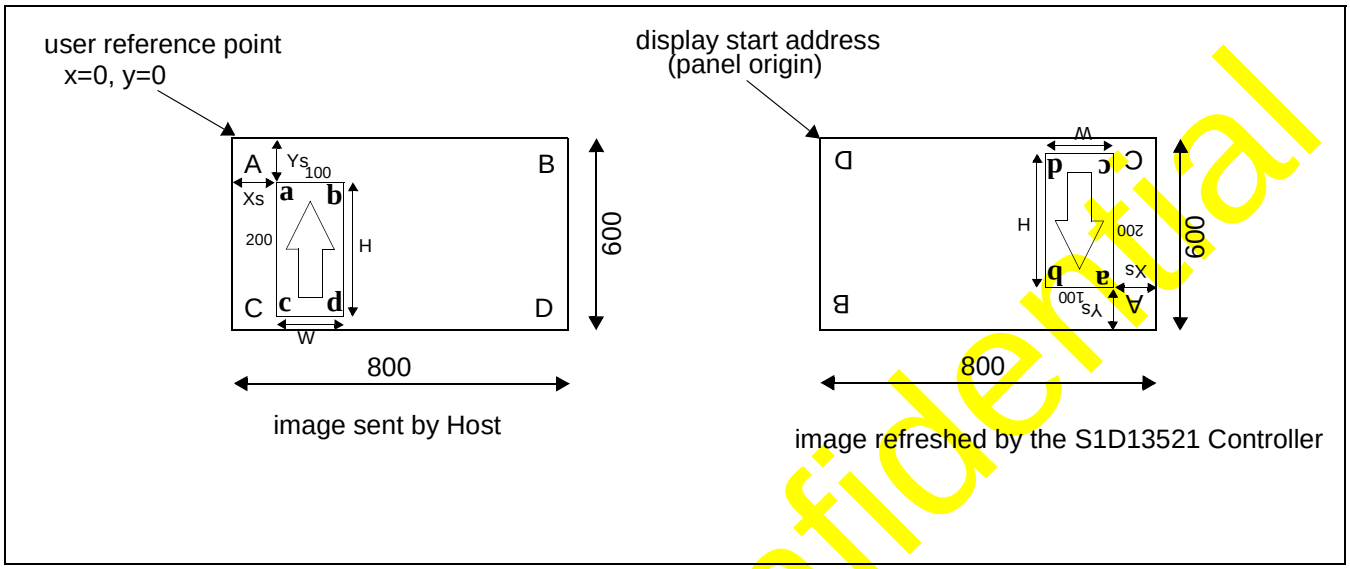


Figure 11-11: Relationship Between the Screen Window Area and the Image Refreshed in 180° Rotation

Programming

There are no special programming requirements other than enabling the rotation (see REG[0140h] bits 9-8). The start address and line offset are automatically calculated by the hardware.

11.5.3 270° Rotation

The following figure shows how the Windowed Area is rotated on the displayed image. The application Window Area is written to the S1D13521 in the following sense: a–b–c–d.

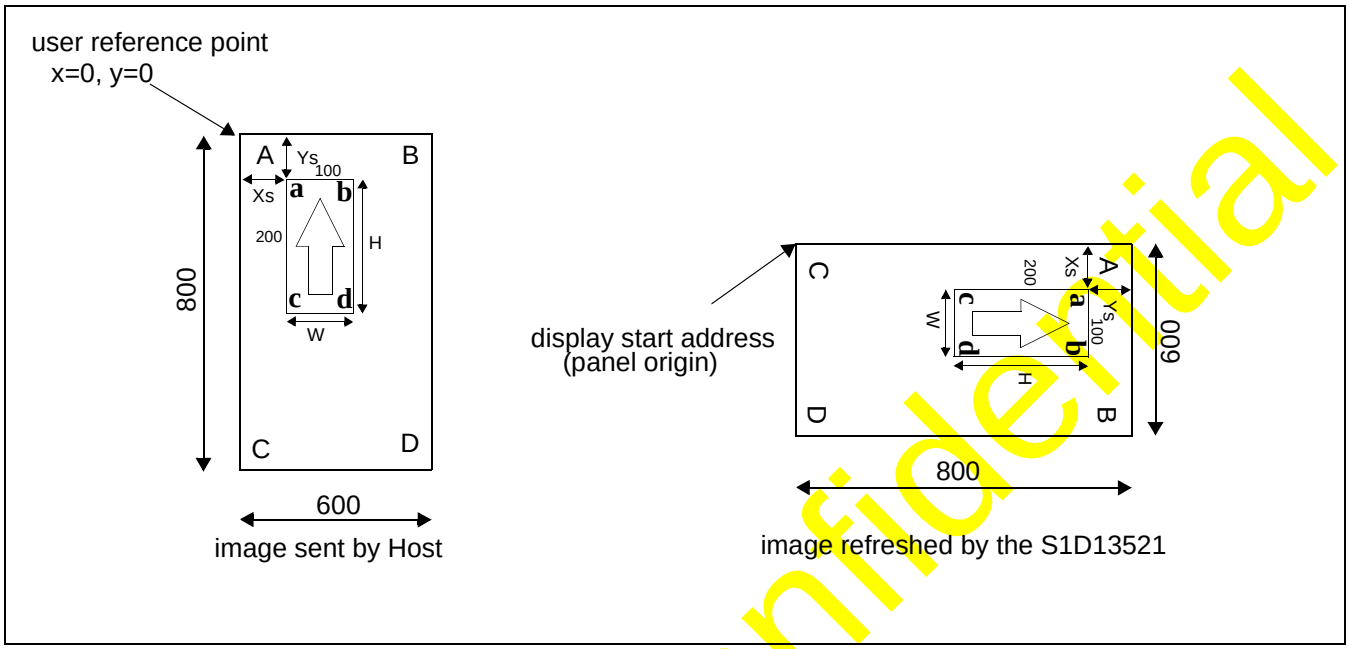


Figure 11-12: Relationship Between the Screen Window Area and the Image Refreshed in 270° Rotation

Programming

There are no special programming requirements other than enabling the rotation (see REG[0140h] bits 9-8). The start address and line offset are automatically calculated by the hardware.

Chapter 12 Display Engine

TBD

Chapter 13 SPI Interface

13.1 Register Descriptions

13.1.1 SPI Flash Chip Select Control Register

The SPI Flash Chip Select Enable bit (REG[0208h] bit 0) is used to assert/deassert the SPICS_L pin. The value programmed to this bit is the inverse of the SPICS_L output. The default value of this bit is 0b (SPICS_L = 1) which disables chip select.

13.1.2 SPI Flash Control Register

The SPI Flash Control Register (REG[0204h]) configures the operation of the SPI Flash Memory interface. It has the following control bits:

- Bit 0 is the SPI Flash Enable bit and is set to 1b to enable the SPI Interface.
- Bits 2-1 are the SPI Flash Clock Phase Select and SPI Flash Clock Polarity Select bits which select the SPICLK phase and polarity. For a summary of the phase and polarity settings, see Table 10-19 “SPI Flash Clock Phase and Polarity,” on page 100.
- Bits 5-3 are the SPI Flash Clock Divide Select bits for programming the SPICLK frequency.
- Bit 6 is the SPI Flash Read Command Select bit and is applicable only when bit 7 is 1b. It selects whether to use Normal Read or Fast Read commands when reading the Serial Flash Memory from the VBUS.
- Bit 7 is the SPI Flash Read Mode bit. When it is 0b, access to the external Serial Flash Memory is through firmware programming of the SPI registers. In this mode, control of the SPI interface engine is given to the SPI interface registers. When it is 1b, the Display Engine has control over the operation of Serial Flash Memory.

13.1.3 SPI Flash Write Data Register

This write only register (REG[0202h]) is used to trigger a byte serial transfer on the SPICLK/SPIO pins. Writing a byte value (with REG[0202h] bit 8 = 1b) to this register causes the byte value to be serial shifted out on SPICLK/SPIO.

13.1.4 SPI Flash Read Data Register

This read only register (REG[0200h]) is used to read byte data received from the SPI interface. In order to read a byte of data into this register, a “dummy” write to REG[0202h] must be performed (with REG[0202h] bit 8 = 0b).

13.1.5 SPI Flash Status Register

This read only register (REG[0206h]) provides status bits indicating the state of the SPI interface engine. The following status bits are available:

- Bit 0 is the SPI Flash Read Data Ready Flag. It is set to 1b whenever a new byte of data has been loaded into the SPI Flash Read Data register, REG[0200h]. This bit is cleared when REG[0200h] is read.
- Bit 1 is the SPI Flash Read Data Overrun Flag. It is set to 1b whenever a new byte of data is loaded into the SPI Flash Read Data register, REG[0200h], and the SPI Flash Read Data Ready Flag (bit 0) is still 1b (indicating that the previous byte has not yet been read out). This bit is cleared by reading REG[0200h].
- Bit 2 is the SPI Flash Write Data Register Empty Flag. It is set to 1b whenever the SPI Flash Write Data Register, REG[0202h], is empty. Writing a byte value to REG[0202h] will initially cause this bit to return 0b. When the byte value is transferred to the serial shift register, this bit is set to 1b again.
- Bit 3 is the SPI Flash Busy Flag. It is set to 1b when the SPI interface engine is busy shifting a byte of data in/out on the SPI interface.

13.2 Flash Memory Accesses using SPI Interface Registers

The following figures show the recommended sequences for accessing the Serial Flash Memory using the SPI interface registers. Before performing instruction sequences, the SPI interface must be configured using the SPI Flash Control Register, REG[0204h]. A Write Enable instruction sequence must have been executed before any Page Program instruction sequence.

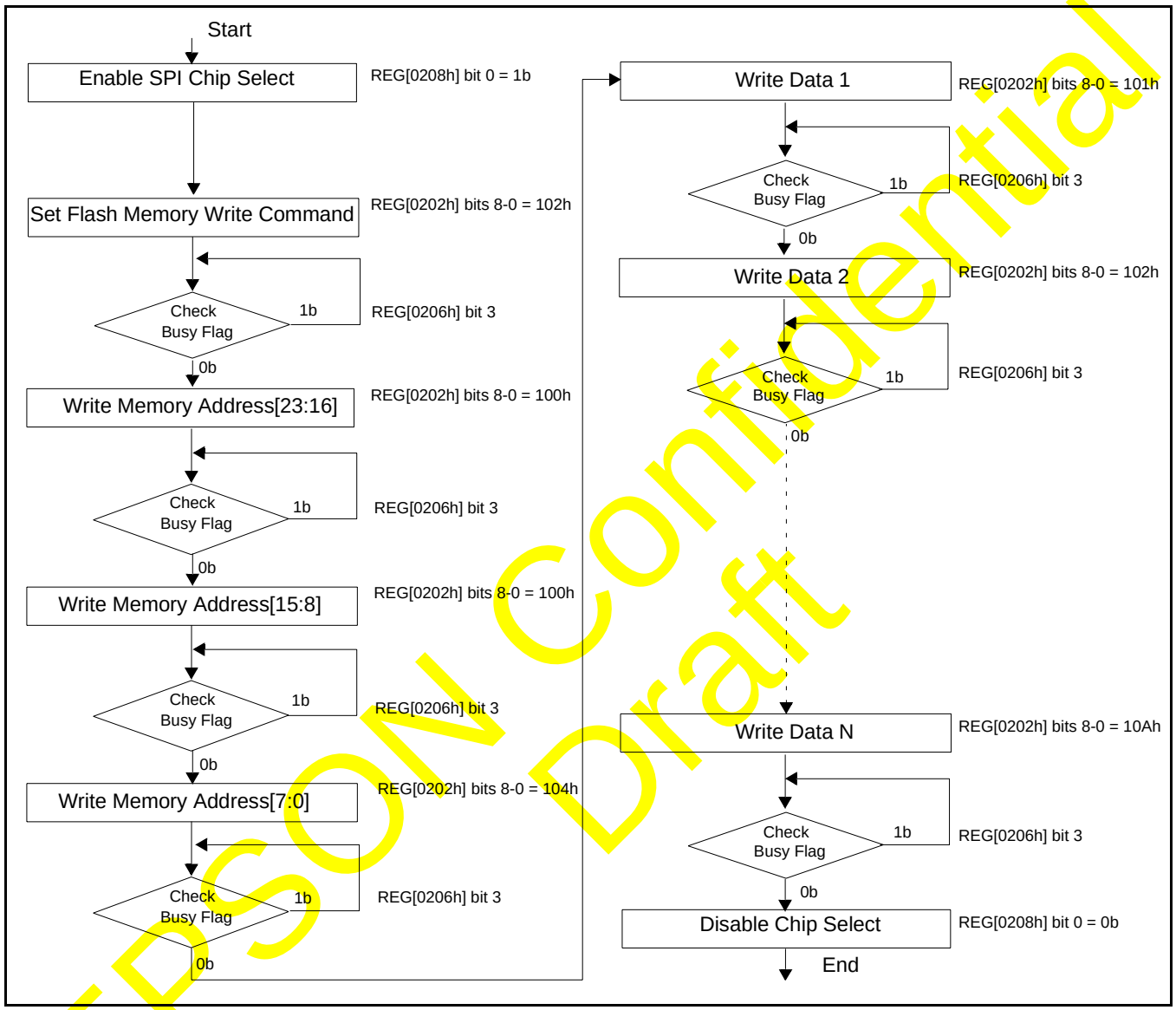


Figure 13-1: Page Program (Write Data) Instruction Sequence

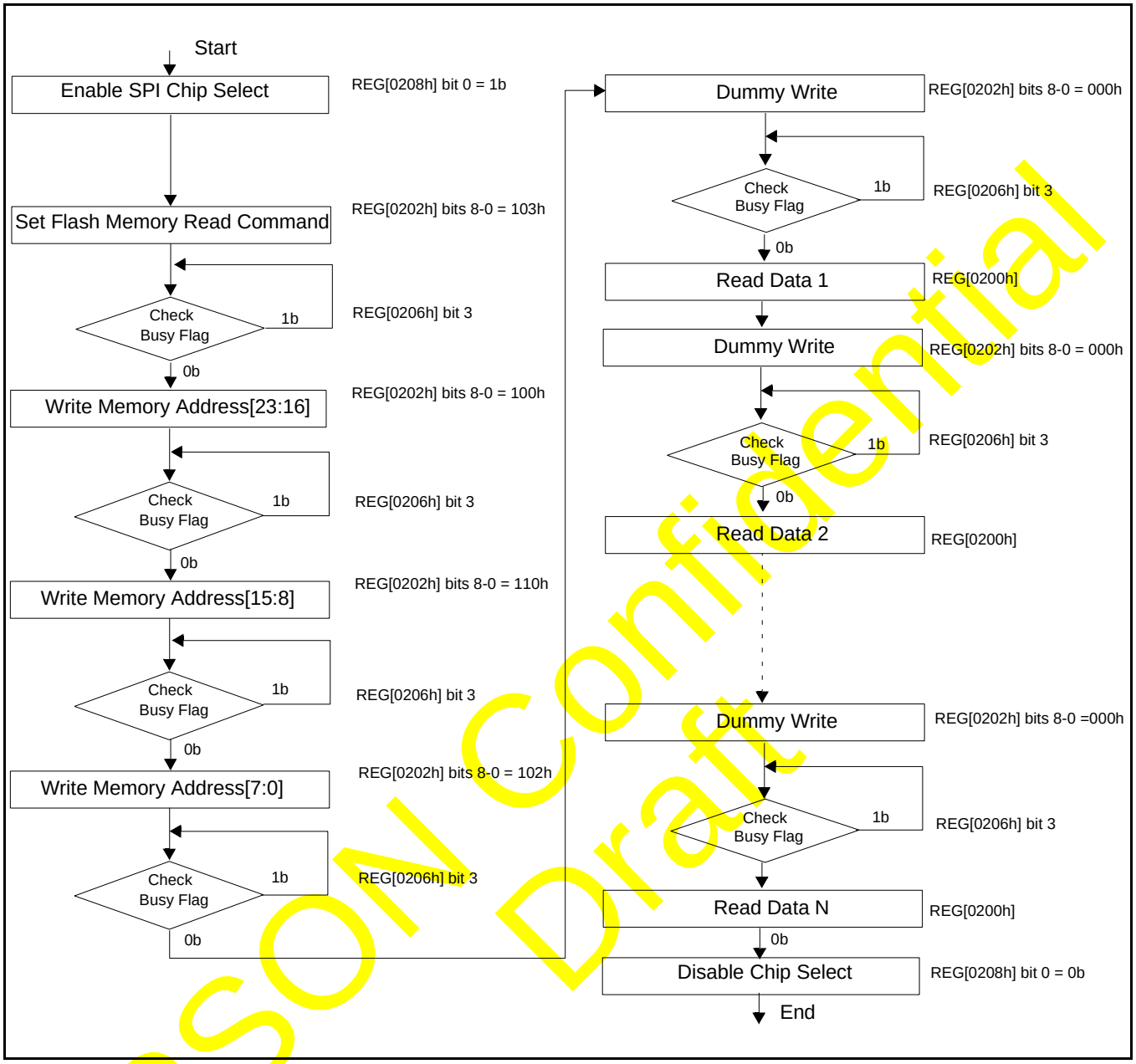


Figure 13-2: Read Data Instruction Sequence

Chapter 14 Firmware Programming Guide

TBD

Chapter 15 Analog Power Supply Considerations

The PLL circuit is an analog circuit which is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of this circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for this circuit be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible.

The following are guidelines which, if followed, will result in cleaner power to the PLL circuit. This will result in a cleaner and more stable clock. Even a partial implementation of these guidelines will give results.

15.1 Guidelines for Analog Power Layout

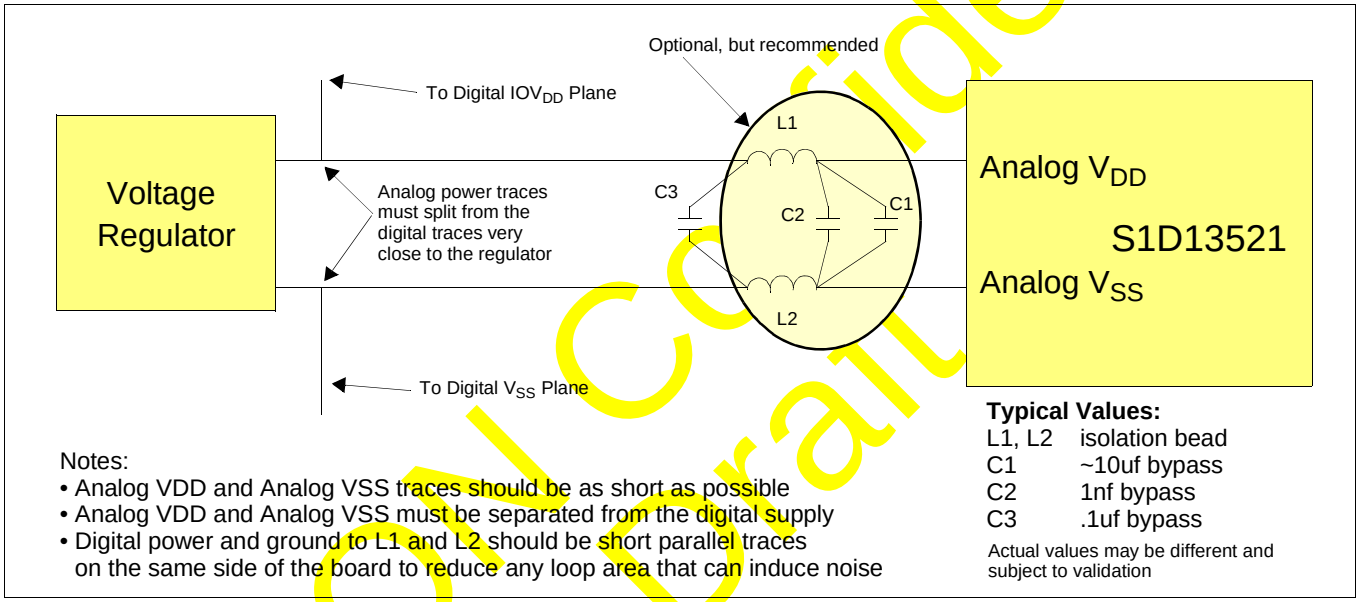


Figure 15-1: Analog Power Layout

- Place the ferrite beads (L1 and L2) parallel to each other with minimal clearance between them. Both bypass caps (C2 and C3) should be as close as possible to the inductors. The traces from C3 to the power planes should be short parallel traces on the same side of the board with just the normal small clearance between them. Any significant loop area here will induce noise. If there is a voltage regulator on the board, try to run these power traces directly to the regulator instead of dropping to the power planes (still follow above rules about parallel traces).
- The analog ground point where bypass cap (C2) connects to the ground isolation inductor (L2) becomes the analog ground central point for a ground star topology. None of the components connect directly to the analog ground pin of the S1D13521 ($PLLV_{SS}$) except for a single short trace from C2 to the $PLLV_{SS}$ pin. The ground side of the large bypass capacitor (C1) should also have a direct connection to the star point.

- The same star topology rules used for analog ground apply to the analog power connection where L2 connects to C2.
- All of the trace lengths should be as short as possible.
- If possible, have all the PLL traces on the same outside layer of the board. The only exception is C1, which can be put on the other side of the board if necessary. C1 does not have to be as close to the analog ground and power star points as the other components.
- If possible, include a partial plane under the PLL area only (area under PLL components and traces). The solid analog plane should be grounded to the C2 (bypass) pad. This plane won't help if it is too large. It is strictly an electrostatic shield against coupling from other layers' signals in the same board area. If such an analog plane is not possible, try to have the layer below the PLL components be a digital power plane instead of a signal layer.
- If possible, keep other board signals from running right next to PLL pin vias on any layer.
- Wherever possible use thick traces, especially with the analog ground and power star connections to either side of C2. Try to make them as wide as the component pads – thin traces are more inductive.

It is likely that manufacturing rules will prohibit routing the ground and power star connections as suggested. For instance, four wide traces converging on a single pad could have reflow problems during assembly because of the thermal effect of all the copper traces around the capacitor pad. One solution might be to have only a single trace connecting to the pad and then have all the other traces connecting to this wide trace a minimum distance away from the pad. Another solution might be to have the traces connect to the pad, but with thermal relief around the pad to break up the copper connection. Ultimately the board must also be manufacturable, so best effort is acceptable.

Chapter 16 Mechanical Data

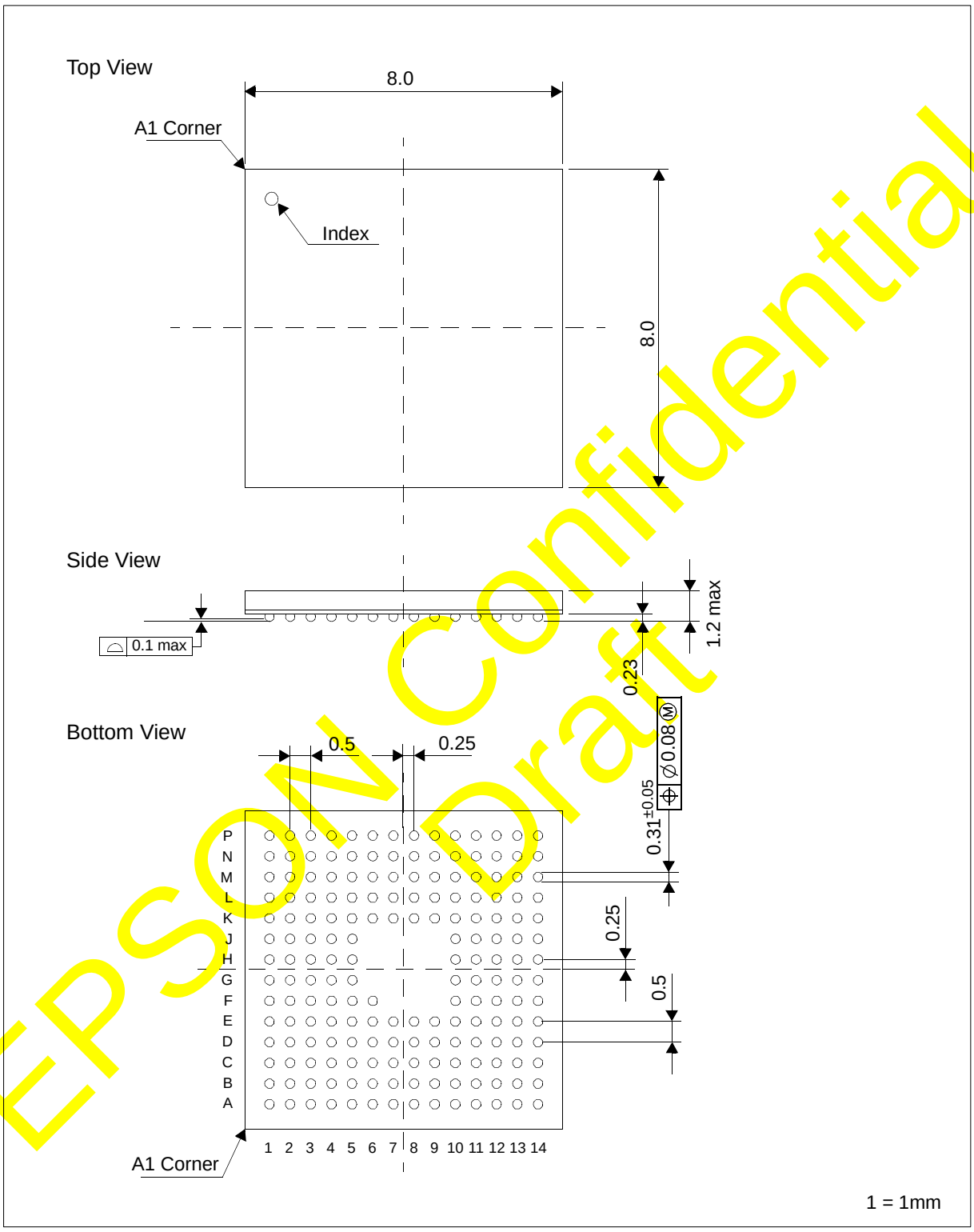


Figure 16-1: PFBGA8UX 181-pin Package

16.1 Thermal Details

The thermal details for the PFBGA8UX 181-pin package are as follows:

θja : 31°C / W (max ±10°C / W)

Chapter 17 References

The following documents contain additional information related to the S1D13521. Document numbers are listed in parenthesis after the document name. All documents can be found at the Epson Research and Development Website at **www.erd.epson.com**.

- S1D13521 Product Brief (X88A-C-001-xx)

Change Record

X88A-A-001-00 Revision 0.05 - Issued: November 7, 2007

- All changes from the previous revision are Red
- section 2.1, changed source/gate driver interface descriptions to include “compatible devices”
- section 2.2, updated 16-bit Host Interface features list with comment about Command Mode and User programmed commands
- section 2.2, removed reference to register mode
- section 2.4, changed Power Management IC description to include “compatible devices”
- section 2.6, added reference to the LM75 in the I2C Thermal Sensor Temperature Reading Features section
- section 2.7, added the Auto Command Sequence Features section
- section 2.9, added Crystal Interface to the Clock Source Features section
- section 2.10, for the Miscellaneous Features section combined the power mode features into “Sleep and Standby Power Save Modes”
- section 3, added basic block diagram
- section 3.1, added typical system implementation
- section 4.2, added ILTR Cell Description
- section 4.2, updated the RESET# state of all pins
- section 4.2, minor edits to clarify the pin descriptions
- section 4.2.7, separated the pin descriptions for SDCE_L[10:9] and SDCE_L[8:0] and added reference on the configurability of the pins
- section 4.2.10, added the OSCI and OSCO pins and pin descriptions to the Miscellaneous section
- section 4.2.10, added the CNF3 pin and pin description to the Miscellaneous section
- section 4.2.11, changed the SDRIOVDD power from “1.65-3.6V” to “1.8/3.3V”, changed the PPIOVDD power from “3.3V” to “1.65-3.6V”, changed the PIOVDD power from “3.3V” to “1.65-3.6V”
- section 4.2.11, added the OSCVDD and OSCVSS pins and pin descriptions to the Power and Ground section
- section 4.2.11, updated the number of balls for each power supply
- section 4.3, added new section summarizing the Configuration Pins
- section 4.4.2 ~ 4.4.3, reworded the table headings for the Source Driver Interface Bitwidth Select and Border Pin Interface Bitwidth Select tables
- section 5.1, added Absolute Maximum Ratings for OSC supply voltage
- section 5.2, added Recommended Operating Conditions for OSC supply voltage
- section 5.2, for the SDRIOVDD Recommended Operating Conditions changed the Min from “3.00” to “2.70”

- section 6.1.1, added OSC option to CLKI Input Requirements
- section 6.1.1, for the Clock Input Requirements table changed the t3 and t4 parameter max values from 5.0ns to 500ps
- section 6.1.1, for the Clock Input Requirements table changed the t5 and t6 parameter min/max values from -300/300ps to -150/150ps
- section 6.1.1, added note 6 about achieving the maximum possible PLL output frequency
- section 6.1.2, reserved the tPJref and tPDuty parameters from he PLL Clock Requirements table
- section 6.2, for the power-on/power-off sequence figures, clarified the maximum voltage allowed
- section 6.4.1, for the 16-bit Host timing updated the min timings for twl, twh, tw2r, tr2w, trl, and trh
- section 6.4.1, for the 16-bit Host timing updated the min timing for tdht from “5ns” to “7ns”
- section 6.5, added Display Timing Register summary and added note
- section 6.5, for the Display Timing, the Line Sync Length formula changed to “((REG[0308h] bits 7-0) x 4) + 2)”
- section 6.5.1, added example Frame Rate Calculation
- section 6.5.2, updated the Source Driver Display Timings
- section 6.5.3, updated the Gate Driver Display Timings
- section 6.6.1, for the PWR[3:0] Transition Sequence figure changed “Frame Clk” to “Line Clk”
- section 6.6.1, for the PWR[3:0] Transition Sequence clarified the text, added values for tu parameter, and removed td parameter
- section 6.6.2, for the PWRCOM Transition Sequence clarified the text, moved t1 in the figure, and added min values to the table
- section 7.1, added OSCI/OSCO to the Clock Tree Diagram
- section 8.1, clarified the S1D13521 power state descriptions
- section 9.1, updated the Host Cycle Sequences section
- section 9.4 ~ 9.5, updated the Command List section
- section 10, unreserved all registers from REG[0000h] ~ REG[0352h]
- REG[000Ah], changed System Status Register from “Read Only” to “Read/Write”
- REG[000Ah] bits 12-10, added the Power Save Status bits and bit description
- REG[000Ah] bit 0, added information to not access the synchronous registers or memory before the PLL output is stable
- REG[0014h] bits 14-8, revised the PLL Setting Example
- REG[0016h], changed default register value from “0000h” to “0002h”
- REG[0108h] bit 3, reserved this bit
- REG[0140h] bit 7, added the Packed Pixel Destination Start Address Select bit and bit description
- REG[0206h], changed default register value from “0000h” to “0004h”

- REG[0220h] ~ REG[0226h], changed the register description to refer to “3-Wire Chip Interface”
- REG[0240h] ~ REG[0244h], changed the register description to refer to “3-Wire Chip Interface”
- REG[0240h], REG[0242h], REG[0244h] bit 8, added the Host Memory Read/Write FIFO Error Interrupt raw status, masked status, and enable bits and bit descriptions
- REG[030Ch] bits 7-0, extended the Source Driver Output Size Select bits from “bits 6-0” to “bits 7-0”
- REG[030Eh] bits 15-11, added the Source Driver SDOED Delay bits and bit descriptions
- REG[030Eh] bit 10, added the Source Driver Double Data Rate Enable bit and bit description
- REG[030Eh] bits 7-4, added the Source Driver SDOEX Delay bits and bit descriptions
- REG[032Ah] bit 8, added the Voltage Control Byte Force Frame Wait bit and bit description
- REG[032Ah] bits 7-4, added the Voltage Control Byte Wait Select bits and bit description
- REG[032Eh], added the LUT Mask register
- REG[0330h] bit 15, for the Display Engine Software Reset bit description added register default value reset comment
- REG[0330h] bits 11-8, added these bits as Reserved bits
- REG[0334h] bit 15, changed the register description to refer to “3-Wire Chip Interface”
- REG[0338h] bit 6, added the Masked LUT Available Status bit and bit description
- REG[033Ah], REG[033Ch], REG[033Eh] bit 13, added the Image Buffer Update Incomplete Interrupt raw status, masked status, and enable bits and bit descriptions
- section 11, minor wording clarifications to the Display Configurations section
- section 11.1, adjusted the Image Area so it is not at the beginning of SDRAM
- section 13, minor wording clarifications to the SPI Interface section
- section 13.1, changed references from “SPICS#” to “SPICS_L”

X88A-A-001-00 Revision 0.04 - Issued: October 19, 2007

- All changes from the previous revision are Red
- section 4.2, updated cell descriptions table and cell descriptions for all pins
- section 4.2.1, updated RESET_L pin description to add cross reference to RESET_L Timing section
- section 4.2.2, removed the reference to CNF0
- section 4.2.2, changed HRDY pin type from “O” to “IO”
- section 4.2.2, clarified some of the Host Interface pin descriptions
- section 4.2.5, for the TI2CC and TI2CD pin descriptions added that they must be connected to PPIOVDD when they are not used
- section 4.2.8, changed PWR0, PWR1, PWR3 pin types from “O” to “IO”
- section 4.2.10, changed CNF1 pin description to be “Reserved. This pin must be connected to HIOVDD.”

- section 4.2.10, for the CNF2 pin description added information that this pin must be connected to VSS
- section 4.2.11, for the PFBGA Pin# column clarified that the number only specifies the number of balls
- section 4.2.11, updated the “power” column for the COREVDD and PLLVDD pins from “1.5V” to “1.8V”
- section 4.3.1, reserved the host pin mapping section
- section 5, replaced DC Characteristics section
- section 5.3, added Electrical Characteristics tables for COREVDD and PLLVDD with TBD values
- section 6.1.1, for the Clock Input Requirements table changed foscmin from “1MHz” to “20MHz” and foscmax from “TBD” to “66.5MHz”
- section 6.1.2, for the PLL Clock section changed the PLL output clock frequency min from “TBD” to “40MHz”
- section 6.1.2, for the PLL Clock section changed the PLL duty cycle from “40/60” to “TBD” and changed the PLL output stable time from “TBD” to “200us”
- section 6.2, added Power-on/off Sequence timing section
- section 6.4, corrected the Host Timing diagram and table to use the correct host pin names
- section 7.1, replaced the Clock Tree Diagram
- section 7.1, reserved clock tree notes
- section 7.2, reserved the PLL Block Diagram
- section 8.1, changed “Init PLL” wait time to “200us”
- section 9 and 10, swapped Host Interface and Registers sections
- section 9, replaced the Host Interface section
- section 10, reserved references to Register Mode
- section 10, added REG[0000h] ~ REG[001Ah] and REG[0200h] ~ REG[020Fh] and updated the register descriptions accordingly
- REG[0010h] bits 5-0, changed PLL input clock range to “20 ~ 66.5MHz”
- REG[0018h] bit 4, added the Pixel Clock Divide Disable bit and bit description
- section 11.2, in the Display Memory Bpp Mode section updated the note that describes 8 bpp mode
- section 11, minor wording clarifications in the Display Configurations section
- section 12, added stub for Display Engine section
- section 13, added SPI Interface section
- section 15, added Analog Power Supply Considerations section
- section 16.1, added Thermal Details for the package
- removed Sales and Technical Support section and added Epson International Sales Operations back page

X88A-A-001-00 Revision 0.03 - Issued: September 10, 2007

- All changes from the previous revision are Red
- section 4.2.4, changed the SPIDCS_L and SPICLK pins from inputs to outputs
- section 4.2.8, updated Dialog DA8590 3-wire signal name and description for the PWR[0] and PWR[3] pins
- section 4.2.10, added the CLKI pin and description
- section 6.4, moved the display timings into the AC Timings section
- section 7.1, updated the clock tree diagram with 3-Wire Serial, Pixel, and I2C Thermal Sensor clock divide register changes
- section 10, various updates and clarifications to the Host Interface section
- section 14, added References section
- section 15, added Sales and Technical Support section

X88A-A-001-00 Revision 0.02 - Issued: July 23, 2007

- All changes from the previous revision are Red
- globally replace “Broadsheet” with “S1D13521”

X88A-A-001-00 Revision 0.01 - Issued: July 19, 2007

- initial draft of the S1D13521 specification

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