

S1D13521 Epson/E-Ink Broadsheet

Hardware Functional Specification

SEIKO EPSON CORPORATION

TICE	

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S1D13521 Hardware Functional Specification (Rev. 0.05)

Chapter 1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13521 EPD Controller. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Display Subsystem Designers and Software Developers.

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We appreciate your comments on our documentation. Please contact us via email at documentation @erd.epson.com.

1.2 Overview Description

EPSON's S1D13521 controller provides a high performance, low cost, solution for current and future E Ink EPDs (Electronic Paper Displays). The controller greatly reduces CPU overhead by providing many functions that were previously handled by the Host.

The S1D13521 allows regional display updates which contribute to very responsive screen changes. The external memory interface is designed with support for 16/32-bit SDRAM bus widths. Additionally, the S1D13521 integrates support for current and future power management chips. All this is achieved with a lower parts cost than previous EPD controllers making the S1D13521 a prefect choice for new designs or design upgrades.



Figure 1-1: S1D13521 Overview

Chapter 2 Features

2.1 Direct Source and Gate Driver for Electrophoretic Display

- Supports up to 4096x4096 resolution
- 2 bpp, 3 bpp, 4 bpp, and 5 bpp grayscale
- Source Driver interfaces to the Micronix MX860 IC and compatible devices
 - Programmable up to 1024 pixels per IC
- Gate Driver interfaces to the Sharp LH1692 and compatible devices

2.2 16-Bit Host Interface

- Indirect 16-bit Host Bus Interface
- Registers can be accessed using Command Mode
- User programmed commands can be used to execute a pre-programmed series of commands

2.3 External Memory SDRAM Interface

- 16/32-bit SDRAM Interface
- Programmable Column Addressing Width
- Maximum operating frequency: 133MHz

2.4 Power Management IC

• Supports 3-wire Dialog DA8590 Active Matrix Power Management IC and compatible devices

2.5 Image Buffer Flexibility

- Host Writes can be rotated counter-clockwise by 90°, 180°, or 270°
- Host Write data input can use packed mode for high-speed transfers
- New image data can be loaded to the image buffer while display updates are in progress

2.6 I2C Thermal Sensor Temperature Reading

- Supports I2C sequence for temperature reading
- Supports National LM75 Digital Temperature Sensor and compatible devices

2.7 Serial Flash Memory Waveform Read

- Serial Flash Memory for Waveform Reads
- High Speed SPI Mode
- Waveform format: E Ink's waveform version 1 and version 2 (voltage controlled waveform)

2.8 Clock Source

- Internal Programmable PLL
- Single MHz clock input: CLKI
- Two terminal Crystal interface: OSCI/OSCO

2.9 Miscellaneous

- Sleep and Standby Power Save Modes
- General Purpose Input/Output pins are available (GPIO[1:0])
 - Interrupt pin associated with selectable GPIO inputs
- Package: PFBGA8UX 181-pin

Chapter 3 Block Diagram





3.1 Typical System Implementation

Chapter 4 Pins

4.1 Pinout Diagram



Figure 4-1: S1D13521 PFBGA8UX 181-pin Pin Mapping (Top View)



Table 4-1: S1D13521 PFBGA8UX 181-pin Pinout (Top View)

4.2 Pin Descriptions

Key:

Pin Types

I	=	Input
0	=	Output
10	=	Bi-Directional (Input/Output)
Р	=	Power pin

RESET# States

Н	=	High level output
L	=	Low level output
Z	=	High Impedance (Hi-Z)
1	=	Pull-up resistor on input
0	=	Pull-down resistor on input
#	=	Active low level

Table 4-2: Cell Descriptions

Item	Description							
IC	High voltage LVCMOS input buffer							
ICS	High voltage LVCMOS Schmitt input buffer							
ICD2	High voltage LVCMOS input buffer with pull-down (100k Ω @3.3V)							
0	High voltage low noise output buffer (4mA@3.3V)							
ОН	High voltage high speed output buffer (4mA@3.3V)							
BC	High voltage LVCMOS low noi <mark>se</mark> bi-directional buffer (4mA@3.3V)							
BCS	High voltage LVCMOS schmitt low noise bi-directional buffer (4mA@3.3V)							
BCD2	High voltage LVCMOS low noise bi-directional buffer (4mA@3.3V) with pull-down (100k Ω @3.3V)							
BCH	High voltage LVCMOS high speed bi-directional buffer (4mA@3.3V)							
ILTR	Low voltage transparent input buffer							
OLTR	Low vol <mark>ta</mark> ge transp <mark>ar</mark> ent output buffer							

4.2.1 Shared Host Interface

Pin Name	Туре	Pin #	Cell	Power	RESET_L State	Description
RESET_L	I		ICS	HIOVDD	_	This active low input sets all internal registers to their default states and forces all signals to their inactive states. When unused, this pin should be connected to HIOVDD. For RESET_L timing details, see Section 6.3, "RESET_L Timing" on page 31.
HIRQ	0		0	HIOVDD	L	This output pin is the Host IRQ.

Table 4-3: Shared Host Interface Pin Descriptions

4.2.2 Host Interface

Pin Name	Туре	Pin #	Cell	Power	RESET_L State	Description
HDB[15:0]	ю		BC	HIOVDD	Z	These pins are the shared command/parameter lines
HWE_L	Ι		ICS	HIOVDD	—	This input pin is the Write Enable signal.
HRD_L	Ι		ICS	HIOVDD	—	This input pin is the Read Enable signal.
HCS_L	Ι		IC	HIOVDD	-	This input pin is the Chip Select signal.
HD/C	I		IC	HIOVDD		This input pin selects between Command (Low) and Parameter (High).
HRDY	ю		BC	HIOVDD	H	This ac <mark>tive high</mark> pin is the Host interface Ready (or WAIT) signal.

Table 4-4: Host Interface Pin Descriptions

4.2.3 SDRAM Interface

Table 4-5: SDRAM Interface Pin Descriptions

Pin Name	Туре	Pin <mark>#</mark>	Cell	Power	RESET_L State	Description
SDRADR[12:0]	0		OH	SDRIOVDD	Ļ	These output pins are the SDRAM Address pins.
SDRBA[1:0]	0		ОН	SDRIOVDD	L	These output pins are the SDRAM Bank Address pins.
SDRCAS#	0		ОН	SDRIOVDD	Н	This output pin is the SDRAM CAS# pin.
SDRRAS#	0		ОН	SDRIOVDD	Н	This output pin is the SDRAM RAS# pin.
SDRRCS#	0		ОН	SDRIOVDD	L	This output pin is the SDRAM CS# pin.
SDRWE#	0		ОН	SDRIOVDD	Н	This output pin is the SDRAM WE# pin.
SDRDQM[3:0]	0		ОН	SDRIOVDD	Н	These output pins are the SDRAM DQM pins.
SDRCKE	0		ОН	SDRIOVDD	Н	This output pin is the SDRAM CKE pin.
SDRCLK	0		ОН	SDRIOVDD	Н	This output pin is the SDRAM CLK pin.
SDRDAT[31:0]	10		BCH	SDRIOVDD	L	These input/output pins are the SDRAM DATA pins.

4.2.4 SPI Master Interface for Serial Flash

Pin Name	Туре	Pin #	Cell	Power	RESET_L State	Description
SPIDCS_L	0		0	PPIOVDD	Н	This output pin is the Slave Chip Select for the SPI interface.
SPICLK	0		0	PPIOVDD	L	This output pin is the Slave Clock for the SPI interface.
SPIDO	0		0	PPIOVDD	L	This pin is the data output for the SPI interface.
SPIDI	Ι		IC	PPIOVDD	—	This pin is the data input for the SPI interface.

Table 4-6: SPI Master Interface Pin Descriptions

4.2.5 I2C Master Interface for Thermal Sensor

Table 4-7: I2C Master Interface Pin Descriptions

Pin Name	Туре	Pin #	Cell	Power	RESET_L State	Description
TI2CC	ю		BCS	PPIOVDD	Z	This input/output pin is the I2C Master Serial Clock. If this pin is not used, it must be connected to PPIOVDD.
TI2CD	ю		BCS	PPIOVDD	Z	This input/output pin is the I2C Master Data. If this pin is not used, it must be connected to PPIOVDD.

4.2.6 Gate Driver Interface

Pin Name	Туре	Pin #	Cell	Power	RESET_L State	Description
GDCLK	0		0	PIOVDD	L	This output pin is the clock for the Gate Driver.
GDSP	0		0	PIOVDD	Н	This output pin is the Gate Driver Start Pulse.
GDOE	0		0	PIOVDD	L	This output pin is the output enable for the Gate Driver.
GDRL	0		0	PIOVDD	L	This output pin is the Gate Driver Right or Left.

Table 4-8: Gate Driver Interface Pin Descriptions

4.2.7 Source Driver Interface

<i>Table 4-9:</i>	Source	Driver	Interface	Pin D	escriptions

Pin Name	Туре	Pin #	Cell	Power	RESET_L State	Description
SDCLK	0		0	PIOVDD	L	This output pin <mark>cis</mark> the clock for the Source Driver.
SDLE	0		0	PIOVDD	L	This output pin is the latch enable for the Source Driver.
SDDO[15:0]	0		0	PIOVDD	L	These are the data output pins for the Source Driver.
SDCE_L[10:9]	0		0	PIOVDD	Н	These output pins are the Source Driver Chip Enables 10-9.
SDCE_L[8:0]	0		0	PIOVDD		These output pins are the Source Driver Chip Enables 8-0. For details on the configurability of these pins, refer to Section 10.3.15, "Display Engine: Driver Configurations" on page 123 (see REG[030Ch]) and Section 6.5.2, "Interpreted Source Driver Timings" on page 36.
SDSHR	0		0	PIOVDD	L	Th <mark>is output</mark> pin is the Source Driver Shift Right Enable.
SDOE	0		0	PIOVDD	L	This output pin is the output enable for the Source Driver.

4.2.8 Power Switches Control Interface

The power control interface signals have dual function pins.

- 1. Power sequence output (default power-on function)
- 2. 3-wire Dialog DA8590 Active Matrix Power Management IC and compatible devices

Table 4-10.	Power	Switches	Control	Interface	Pin D	escriptions
<i>1 ubie</i> 4-10.	rower	Swiiches	Comiroi	interjace	I m D	escriptions

Pin Name	Туре	Pin #	Cell	Power	RESET_L State	Description
PWR0/ DAPWRALL	Ю		BC	PWIOVDD	L	 These input/output pins have multiple functions. Power Control Signal 0 (PWR0). For timing details, see Section 6.6.1, "Power Pin Transition Sequence for PWR[3:0]" on page 43. 3-wire Power All Pin output (DAPWRALL)
PWR1/DACLK	Ю		BC	PWIOVDD	L	 These input/output pins have multiple functions. Power Control Signal 1 (PWR1). For timing details, see Section 6.6.1, "Power Pin Transition Sequence for PWR[3:0]" on page 43. 3-wire Serial Clock (DACLK)
PWR2/DADIO	Ю		BC	PWIOVDD	L	 These input/output pins have multiple functions. Power Control Signal 2 (PWR2). For timing details, see Section 6.6.1, "Power Pin Transition Sequence for PWR[3:0]" on page 43. 3-wire data tri-state input/output (DADIO)
PWR3/ DACEB	Ю		BC	PWIOVDD		 These input/output pins have multiple functions. Power Control Signal 3 (PWR3). For timing details, see Section 6.6.1, "Power Pin Transition Sequence for PWR[3:0]" on page 43. 3-wire active low enable (DACEB)
PWRCOM	0		0	PWIOVDD	L	Display Common Power Signals. For timing details, see Section 6.6.2, "Power Pin Transition Sequence for PWRCOM" on page 44.

4.2.9 Display Border Power Interface

Table 4-11: Display Border Power Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET_L State	Description
BDR[3:0]	9		0	PWIOVDD	L	These output pins are the Display Border Power Signals.

4.2.10 Miscellaneous

Pin Name	Туре	Pin #	Cell	Power	RESET_L State	Description
CLKI	I		ICS	HIOVDD	_	This pin is the clock input. For details on the clock structure, see Section Chapter 7, "Clocks" on page 45.
OSCI	I		ILTR	OSCVDD	_	This pin is the input for the 2-terminal crystal interface. When the internal oscillator is not used, this pin must be connected to OSCVDD. For details on the clock structure, see Section Chapter 7, "Clocks" on page 45.
OSCO	ο		OLTR	OSCVDD	н	This pin is the output for the 2-terminal crystal interface. When the internal oscillator is not used, this pin must be left unconnected. For details on the clock structure, see Section Chapter 7, "Clocks" on page 45.
CNF[3:0]	I		IC	HIOVDD	_	These input pins are used for configuring the S1D13521 and must be connected to either HIOVDD or VSS. The states of these pins are latched at RESET_L. For a sum mary of configuration options, see Section 4.3, "Configuration Pins" on page 22.
GPIO[1:0]	ю		BCD2	HIOVDD	Z	These are the General Purpose Input/Output pins.
TESTEN	Ι		ICD2	HIOVDD	_	This input pin is the Test Enable pin and is used for production test only. This pin should be left unconnected for normal operation.
SCANEN	I		ICD2	HIOVDD	7	This input pin is the Scan Enable pin and is used for production test only. This pin should be left unconnected for normal operation.
VCP	0		OLTR	PLLVDD	T	This output pin is for production test only and must be left unconnected for normal operation.

Table 4-12: Miscellaneous Pin Descriptions

4.2.11 Power and Ground

Pin Name	Туре	PFBGA Pin#	Cell	Power	RESET_L State	Description
HIOVDD	Р	2 balls	Р	1.65-3.6V	—	IO power supply for the Host interface
SDRIOVDD	Р	4 balls	Р	1.8/3.3V	—	IO power supply for the SDRAM interface
PPIOVDD	Р	1 ball	Р	1.65-3.6V	—	IO power supply for the SPI and I2C interface
PWIOVDD	Р	1 ball	Р	1.65-3.6V	—	IO power supply for power switch & Display border control
PIOVDD	Р	2 balls	Р	1.65-3.6V	—	IO power supply for Source and Gate Driver
COREVDD	Р	6 balls	Р	1.8V	—	Core power supply
VSS	Р	15 balls	Р	0	_	GND for HIOVDD, SDRIOVDD, SPIOVDD, PIOVDD, TSIOVDD, PWIOVDD, DBIOVDD, PIOVDD, and COREVDD
PLLVDD	Р	1 ball	Р	1.8V	—	PLL power supply
PLLVSS	Р	1 ball	Р	0	—	GND for PLLVDD
OSCVDD	Р	1 ball	Р	1.8V	—	OSC power supply
OSCVSS	Р	1 ball	Р	0	—	GND for OSCVDD

Table 4-13: Power And Ground Pin Descriptions

4.3 Configuration Pins

The S1D13521 has four configuration pins, CNF[3:0], which should be pulled high or low based on the following table.

Table 4-14: Configuration Pin Summary

CNF[3:0]	1 (connected to HIOVDD)	0 (connected to VSS)
CNF3	HRDY only driven when HCS_L is asserted	HRDY is always driven
CNF2	OSCI/OSCO is the source for the Input Clock.	CLKI is the source for the Input Clock.
CNF1	Reserved. This pin must be connected to HIO	/DD.
CNF0	Reserved. This pin must be connected to VSS.	

4.4 Pin Mapping

4.4.1 Source Driver Interface

The Source Driver output width is dependent on the Pixel Output Count Select bit (see REG[030Ch] bit 11).

Bin Nama	Pixel Output C (4 pixels p	ount Select = 0 er SDCLK)	Pixel Output Count Select = 1 (8 pixels per SDCLK)		
	2-bit Voltage Level Control	4-bit Voltage Level Control	2-bit Voltage Level Control	4-bit Voltage Level Control	
SDCLK	SDCLK	SDCLK	SDCLK		
SDLE	SDLE	SDLE	SDLE		
SDDO[1:0]	Pixel 0[1:0]	Pixel 0[1:0]	Pixel 0[1:0]		
SDDO[3:2]	Pixel 1[1:0]	Pixel 0[2:3]	Pixel 1[1:0]		
SDDO[5:4]	Pixel 2[1:0]	Pixel 1[1:0]	Pixel 2[1:0]		
SDDO[7:6]	Pixel 3[1:0]	Pixel 1[2:3]	Pixel 3[1:0]		
SDDO[9:8]	driven 0	Pixel 2[1:0]	Pixel 4[1:0]	No Supported Mode	
SDDO[11:10]	driven 0	Pixel 2[2:3]	Pixel 5[1:0]		
SDDO[13:12]	driven 0	Pixel 3[1:0]	Pixel 6[1:0]		
SDDO[15:14]	driven 0	Pixel 3[2 <mark>:3</mark>]	Pixel 7[1:0]		
SDCE_L[10:0]	SDCE_L[10:0]	SDCE_L[10:0]	SDCE_L[10:0]		
SDSHR	SDSHR	SDSHR	SDSHR		
SDOE	SDOE	SDOE	SDOE		

Table 4-15: Source Driver Interface Bitwidth Select

4.4.2 Border Pin Interface

Tab <mark>le</mark> 4-16:	Border Pin	Inte	<mark>r</mark> face	Bitwidth Select

Pin Name	2-bit Voltage Level Control	4-bit Voltage Level Control
BDR[1:0]	Border Value[1:0]	Border Value[1:0]
BDR[3:2]	Driven 0	Border Value[2:3]

Chapter 5 D.C. Characteristics

5.1 Absolute Maximum Ratings

Table 5-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	
Core V _{DD}	Core Supply Voltage	V _{SS} - 0.3 ~ 2.5	V	
PLL V _{DD}	PLL Supply Voltage	V _{SS} - 0.3 ~ 2.5	V	
OSC V _{DD}	OSC Supply Voltage	V _{SS} - 0.3 ~ 2.5		
HIO V _{DD}	Host IO Supply Voltage	V _{SS} - 0.3 ~ 4.0	V	
PIO V _{DD}	Gate/Source IO Supply Voltage	V _{SS} - 0.3 ~ 4.0	V	
SDRIO V _{DD}	SDRAM IO Supply Voltage	V _{SS} - 0.3 ~ 4.0	V	
PPIO V _{DD}	SPI and I2C IO Supply Voltage	V _{SS} - 0.3 ~ 4.0	V	
PWIO V _{DD}	Power Switch Control IO Supply Voltage	V _{SS} - 0.3 ~ 4.0	V	
V _{IN}	Input Signal Voltage	V _{SS} - 0.3 ~ *IO V _{DD} + 0.5	V	
V _{OUT}	Output Signal Voltage	V _{SS} - 0.3 ~ *IO V _{DD} + 0.5	V	
I _{OUT}	Output Signal Current	±10	mA	
T _{STG}	Storage Temperature	-6 <mark>5 ~</mark> 150	°C	

Note

 $V_{SS} = 0 V$ Core V_{DD} , PLL V_{DD} , OSC $V_{DD} \le *IOV_{DD}$

5.2 Recommended Operating Conditions

Table 5-2: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Тур	Max	Units
Core V _{DD}	Core Supply Voltage	V _{SS} = 0 V	1.65	1.80	1.95	V
PLL V _{DD}	PLL Supply Vo <mark>lt</mark> age	V _{SS} = 0 V	1.65	1.80	1.95	V
OSC V _{DD}	OSC Supply Voltage	V _{SS} = 0 V	1.65	1.80	1.95	V
HIO V _{DD}	Host IO Supply Voltage	V _{SS} = 0 V	1.65	_	3.60	V
PIO V _{DD}	Gate/Source IO Supply Voltage	$V_{SS} = 0 V$	1.65	_	3.60	V
		$V_{SS} = 0 V$	1.65	1.80	1.95	V
SPICE APP	Solution to Supply Voltage	$V_{SS} = 0 V$	2.70	3.30	3.60	V
	SPI and I2C IO Supply Voltage	$V_{SS} = 0 V$	1.65	_	3.60	V
	Power Switch Control IO Supply Voltage	V _{SS} = 0 V	1.65	_	3.60	V
V _{IN}	Input Voltage	_	V_{SS}		*IO V _{DD}	V
T _{OPR}	Operating Temperature	_	-40	25	85	°C

5.3 Electrical Characteristics

Symbol	Parameter	Condition	Min	Тур	Max	Units
I _{DDS}	Quiescent Current	Quiescent Conditions	—	TBD	—	μA
I _{IZ}	Input Leakage Current	—	-5	—	5	μA
I _{OZ}	Output Leakage Current	—	-5	—	5	μA
I _{ОН}	High Level Output Current	$IOV_{DD} = min$ $V_{OH} = IO V_{DD} - 0.4 V$	-2	_	-	mA
I _{OL}	Low Level Output Current	$IOV_{DD} = min$ $V_{OL} = 0.4 V$	2	—	• /	mA
V _{IH}	High Level Input Voltage	LVCMOS Level IO V _{DD} = max	1.27	-	10 V _{DD} + 0.3	V
V _{IL}	Low Level Input Voltage	LVCMOS Level IO V _{DD} = min	-0.3		0.57	V
V _{T+}	Positive Trigger Voltage	LVCMOS Schmitt	0.58		1.46	V
V _{T-}	Negative Trigger Voltage	LVCMOS Schmitt	0.42		1.26	V
V _H	Hysteresis Voltage	LVCMOS Schmitt	0.17	_	—	V
R _{PU}	Pull-Up Resistance	$V_{IN} = 0 V$	96	240	600	kΩ
R _{PD}	Pull-Down Resistance	V _{IN} = IO V _{DD}	96	240	600	kΩ
Cl	Input Pin Capacitance	f = 1MHz, IO V _{DD} = <mark>0</mark> V			6	pF
C _O	Output Pin Capacitance	f = 1MHz, IO V _{DD} = 0V	<u> </u>	—	6	pF
C _{IO}	Bi-Directional Pin Capacitance	f = 1MHz, IO V _{DD} = 0V	-	—	6	pF

Table 5-3: Electrical Characteristics for IO $V_{DD} = 1.8V \pm 0.15V$

Table 5-4: Electrical Characteristics for IO $V_{DD} = 2.5V \pm 0.2V$

Symbol	Parameter	Condition	Min	Тур	Max	Units
I _{DDS}	Quiescent Current	Quiescent Conditions		TBD		μA
I _{IZ}	Input Leakage Current		-5	_	5	μA
I _{OZ}	Output Leakage Current	-	-5	_	5	μA
I _{ОН}	High Level Output Current	IOV _{DD} = min V _{OH} = IO V _{DD} - 0.4 V	-3	_	—	mA
I _{OL}	Low Level Output Current	$V_{OL} = min$ $V_{OL} = 0.4 V$	3			mA
V _{IH}	High Level Input Voltage	LVCM <mark>OS Le</mark> vel IO V _{DD} = max	1.7	_	IO V _{DD} + 0.3	V
V _{IL}	Low Level Input Voltage	LVCMOS Level IO V _{DD} = min	-0.3	_	0.7	V
V _{T+}	Po <mark>si</mark> tive Trigger Voltage	LVCMOS Schmitt	0.92	_	1.89	V
V _{T-}	Negative Trigger Voltage	LVCMOS Schmitt	0.58	_	1.48	V
V _H	Hysteresis Voltage	LVCMOS Schmitt	0.23	_	—	V
R _{PU}	Pull-Up Resistance	V _{IN} = 0 V	70	140	350	kΩ
R _{PD}	Pull-Down Resistance	V _{IN} = IO V _{DD}	70	140	350	kΩ
C _I	Input Pin Capacitance	f = 1MHz, IO V _{DD} = 0V	—	_	6	pF
C _O	Output Pin Capacitance	f = 1MHz, IO V _{DD} = 0V	—	_	6	pF
C _{IO}	Bi-Directional Pin Capacitance	$f = 1MHz$, IO $V_{DD} = 0V$			6	pF

Symbol	Parameter	Condition	Min	Тур	Max	Units
I _{DDS}	Quiescent Current	Quiescent Conditions	—	TBD	—	μA
I _{IZ}	Input Leakage Current	—	-5	—	5	μΑ
I _{OZ}	Output Leakage Current	—	-5	—	5	μΑ
I _{OH}	High Level Output Current	$IOV_{DD} = min$ $V_{OH} = IO V_{DD} - 0.4 V$	-4	_		mA
I _{OL}	Low Level Output Current	$IOV_{DD} = min$ $V_{OL} = 0.4 V$	4	—	-	mA
V _{IH}	High Level Input Voltage	LVCMOS Level IO V _{DD} = max	2.2	—	10 V _{DD} + 0.3	V
V _{IL}	Low Level Input Voltage	LVCMOS Level IO V _{DD} = min	-0.3	_	0.8	V
V _{T+}	Positive Trigger Voltage	LVCMOS Schmitt	1.2	-	2.52	V
V _{T-}	Negative Trigger Voltage	LVCMOS Schmitt	0.75		1.98	V
V _H	Hysteresis Voltage	LVCMOS Schmitt	0.3			V
R _{PU}	Pull-Up Resistance	$V_{IN} = 0 V$	50	100	240	kΩ
R _{PD}	Pull-Down Resistance	V _{IN} = IO V _{DD}	50	100	240	kΩ
Cl	Input Pin Capacitance	f = 1MHz, IO V _{DD} = 0V		<u> </u>	6	pF
C _O	Output Pin Capacitance	f = 1MHz, IO V _{DD} = 0V		—	6	pF
C _{IO}	Bi-Directional Pin Capacitance	$f = 1MHz$, IO $V_{DD} = 0V$		—	6	pF

Table 5-5: Electrical Characteristics for IO $V_{DD} = 3.3V \pm 0.3V$

Table 5-6: Electrical Characteristics for CORE V_{DD}

Symbol	Parameter	Condition	Min	Тур	Мах	Units
I _{DDS}	Quiescent Current	Quiescent Conditions		TBD	—	μA
I _{IZ}	Input Leakage Current		-5	—	5	μA
I _{OZ}	Output Leakage Current		-5	—	5	μA

Table 5-7: Electrical Characteristics for PLL V_{DD}

Symbol	Parameter	Condition	Min	Тур	Max	Units
I _{DDS}	Quiescent Cu <mark>rre</mark> nt	Quiescent Conditions	—	TBD	—	μΑ
I _{IZ}	Input Leakage Current	— <u> </u>	-5	_	5	μΑ
I _{OZ}	Output Leakage Current	—	-5		5	μΑ

Chapter 6 A.C. Characteristics

Conditions: TBD

6.1 Clock Timing

6.1.1 Input Clocks



Figure 6-1 Clock Input Required (CLKI)

Symbol	Parameter	Min	Тур	Max	Units
	Input clock frequency of CLKI when PLL used for System Clock (see Note 6)	20	_	66.5	MHz
f _{OSC}	Input clock frequency of CLKI when CLKI used for System Clock	0	_	TBD	MHz
	Input clock frequency of OSC when PLL used for System Clock (see Note 6)	24	_	27	MHz
t _{OSC}	Input clock period		1/f _{OSC}	—	μs
t1	Input clock pulse width high (see Note 5)	0.4t _{OSC}	_	0.6t _{OSC}	μs
t2	Input clock pulse width low (see Note 5)	0.4t _{OSC}	_	0.6t _{OSC}	μs
t3	Input clock rise time (10% - 90%)		_	500	ps
t4	Input clock fall time (90% - 10%)		_	500	ps
t5	Input clock period jitter (see notes 2 and 4)	-150		150	ps
t6 (see note 1)	Input clock cycle jitter (see notes 3 and 4)	-150		150	ps

Table 6-1 Clock Input Requirements

1. $t6 = 2 \times t_{OSC}$

- 2. The input clock period jitter is the displacement relative to the center period (reciprocal of the center frequency).
- 3. The input clock cycle jitter is the difference in period between adjacent cycles.
- 4. The jitter characteristics must satisfy both the t5 and t6 characteristics
- 5. Input Duty cycle is not critical and can be 40/60
- To achieve the maximum possible PLL output frequency, the input source frequency must be evenly divisible into 133 MHz. For further details on programming the PLL, see Section 10.3.2, "Clock Configuration Registers" on page 83.

6.1.2 PLL Clock

The PLL circuit is an analog circuit and is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible. The jitter of the input clock waveform should be as small as possible.



Figure 6-2: PLL Start-Up Time

Table 6-2:	PLL	Clock	Red	auir	ements	
1 11010 0 2.	1 111	010010	1100	10000	envenus	

Symbol	Parameter	Min	Max	Units
f _{PLL}	PLL output clock frequency	40	133	MHz
t _{PStal}	PLL output stable time		200	μs

6.2 Power Supply Sequence

6.2.1 Power-On Sequence





Table 6-3: Power-On Sequ <mark>e</mark> nc
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Symbol	Parameter	Min	Мах	Units
t1	HIOVDD, SDRIOVDD, PPIOVDD, PWIOVDD, PIOVDD on delay from COREVDD, PLLVDD on	0	500	ms
t2	RESET_L deasserted from HIOVDD, SDRIOVDD, PPIOVDD, PWIOVDD, PIOVDD on	50	_	ns

6.2.2 Power-Off Sequence



Figure 6-4: Power-Off Sequence

Table 6-4: Power-Off Sequence

Symbol	Parameter	Min	Max	Units
t1	COREVDD, PLLVDD off delay from HIOVDD, SDRIOVDD, PPIOVDD, PWIOVDD, PIOVDD off	0	500	ms

6.3 RESET_L Timing



Table 6-5 S1D13521 RESET_L Timing

Symbol	Parameter		Min	Max	Units
t1	Active Reset Pulse Width		1	_	CLKI

6.4 Host Interface Timing



6.4.1 16-bit Host Interface Timing

Figure 6-6: 16-bit Host Input A.C. Characteristics

Signal	Symbol	Parameter	Min	Max	Unit	Description
	t _{ast}	Address setup time (read/write)	1	_	ns	
HD/C	t _{wah}	Address hold time (write)	5	_	ns	
	t _{rah}	Address hold time (read)	29	_	ns	
	t _{wcs}	Chip Select setup time (write)	t _{wl}	_	ns	
	t _{rcs}	Chip Select setup time (read)	t _{rl}	_	ns	
100_L	t _{ch}	Chip Select hold time (read/write)	0	— 🔶	ns	
	t _{csf}	Chip Select Wait time (read/write)	1		ns	
	t _{wl}	Pulse low duration	2	— —	Ts	
HWE_L	t _{wh}	Pulse high duration	1		Ts	
	t _{w2r}	HWE_L rising edge to HRD_L falling edge	2		Ts	
	t _{r2w}	HRD_L rising edge to HWE_L falling edge	1		Ts	
HRD_L	t _{rc}	Read cycle	t _{rl} + t _{rh}		ns	
	t _{rl}	Pulse low duration	5		Ts	
	t _{rh}	Pulse high duration for Registers		<u> </u>	Ts	
		Pulse high duration for Memory and LUT	2		Ts	
	t _{dst}	Write data setup time	4	_	ns	
	t _{dht}	Write data hold time	7	_	ns	
	t _{rodh}	Read data hold time from HRD_L rising edge	11	_	ns	
	t _{rrdz}	HRD_L rising edge to HDB[15:0] Hi-Z	<u> </u>	31	ns	
	t _{codh}	Read data hold time from HCS_L rising edge	1	_	ns	
	t _{crdz}	HCS_L rising edge to HDB[15:0] Hi-Z		8	ns	
HDB[15:0]		HRD_L falling edge to HDB[15:0] valid for Registers		16	ns	CI = 30pE
	t.	HRD_L falling edge to HDB[15:0] valid for Memory		5SYSCLK + 19	ns	OL-SOPI
	۲dv	HRD_L falling edge to HDB[15:0] valid for Registers	_	11	ns	CL – 8pF
		HRD_L falling edge to HDB[15:0] valid for Memo <mark>ry</mark>	_	5SYSCLK + 14	ns	
	t	HRD_L falling edge to HDB[15:0] driven	4		ns	CL=30pF
	⁴ rdd	HRD_L falling edge to HDB[15:0] driven	3		ns	CL = 8pF

Table 6-6: 16-bit Host Input A.C. Characteristics



6.5 Display Timings

The display frame settings are based on the display timing configuration registers as shown below.

Table 6-7: Display Timing Registers

Display Timing Name	Registers and Bits	Units
Frame Sync Length	(REG[0302h] bits 7-0) + 1	Lines
Frame Begin Length	REG[0304h] bits 7-0	Lines
Frame End Length	REG[0304h] bits 15-8	Lines
Frame Data Length	REG[0300h] bits 12-0	Lines
Line Sync Length	((REG[0308h] bits 7-0) x 4) + 2	Pixels
Line Begin Length	(REG[030Ah] bits 7-0) x 4	Pixels
Line End Length	(REG[030Ah] bits 15-8) x 4	Pixels
Line Data Length	REG[0306h] bits 12-0	Pixels



Note

To allow extra pixel lines to be hidden under the Line End Length, the display timing values should be programmed such that the following formula is valid.

 $(Line Data Length + Line End Length) \geq Source Driver Output Total Count$

6.5.1 Frame Rate Calculation Guide

The Frame Rate can be determined using the following formulas.

 $PixelClkFrequency = \frac{133Mhz}{PixelClkDivideSelected(REG[0018])}$

SourceDriverClkFrequency = <u>PixelPerClockOutputSelect(REG[030C - Bit11])</u>

HorizontalTotalPixel = LineSyncLength + LineBeginLength + LineDataLength + LineEndLength

GateDriverGDCLKFrequency = $\frac{SourceDriverClkFrequency}{HorizontalTotalPixel}MHz$

VerticalTotalLines = FrameSyncLength + FrameBeginLength + FrameDataLength + FrameEndLength

FrameRate = GDCLKFrequency VerticalTotalLines

The following shows example values for an 800x600 display.

Pixel Clock Divide Select	7		Internal Clock	133	MHz
Pixel Clock Frequency	16.625	MHz	Divide Selected	8	
SDCLK Frequency	8.3125	MHz			

Table 6-8 :	Frame Rate	Calculation	Examp	le f <mark>or</mark>	800x600
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Register Settings				
Frame Sync Length	4			
Frame Begin Length	4			
Frame End Length	5			
Frame Data Length	600			

Line Sync Len <mark>gt</mark> h	10	
Line Begin Len <mark>gth</mark>	20	
Line End Length	40	
Line Data Length	800	

GDCLK High Time	230.5	SDCLKs
GDCLK Low Time	40	SDCLKs
GDCLK Frequency	30.73013	KHz

Total Lines	614	Lines
Frame Rate	50.04907	Hz

6.5.2 Interpreted Source Driver Timings

The following figure shows an example Source Driver connection using a Micronix MX860 (268 outputs per driver).



Figure 6-8: Source Driver Connection Example using MX860


Source Driver Display Timing 1: 4 Pixel per Clock Output

Figure 6-9: Source Driver Display Timing for 4 Pixel per clock Output

Table 6-9: Source	Driv	er Display	Timing for	<u>4</u>	Pixe	l Per	Clock Output

Timing	Description	Value	Min	Max
t1	Dual Pixel Clock Period	From Pixel Clock Divide	12ns	—
t2	SDCLK Perio <mark>d f</mark> or 4 Pixel <mark>p</mark> er clock	2 x t1	24ns	—
t3	Line Start Length	(Line Start Length ÷ 4 x t2) + t1	3 x t1	_
t4	Source Driver Latch Enable High time	t3 - t1	t3 - t1	t3 - t1
t5	SDLE deassert to First Data output	(Line Begin Length ÷ 4 x t2)	0	
t6	Source Driver Output Enable before Data Valid	1 x t2	1 x t2	1 x t2
t7	Data Output Time	Line Data Length ÷ 4 x t2	2 x t2	
t8	SDOE deassert time from last data output	(Line End Length ÷ 4 x t2) - t1	1 x t2	
t9	Gate Driver Clock positive edge	1 x t1	1 x t1	1 x t1
t10	Gate Driver Clock negative edge	1 x t1	1 x t1	1 x t1
t11	Gate Driver Clock High Time	((Line Start + Line Begin + Line Data Length) ÷ 4 x t2) + t10	1 x t2	_
t12	Gate Driver Clock Low Time	(Line End Length ÷ 4 x t2) - t10	1 x t2	_

Source Driver Display Timing 2: 8 Pixel per Clock Output



Figure 6-10: Source Driver Display Timing for 8 Pixel per clock Output

Table 6-10: Source Driver Display Timing for 8 Pixel Per Clock Output

Timing	Description	Value	Min	Max
t1	Dual Pixel Clock Period	From Pixel Clock Divide	12ns	—
t2	SDCLK Period f <mark>or</mark> 8 Pixel p <mark>er</mark> clock	4 x t1	48ns	—
t3	Line Start Length	Line Start Length ÷ 8 x t2) + t1	3 x t1	—
t4	Source Driver Latch Enable High time	t3 - t1	t3 - t1	t3 - t1
t5	SDLE deassert to First Data output	(Line Begin Length ÷ 8 x t2)	0	—
t6	Source Driver Output Enable before Data Valid	1 x t2	1 x t2	1 x t2
t7	Data Output Time	Line Data Length ÷ 8 x t2	2 x t2	—
t8	SDOE deassert time from last data output	(Line End Length ÷ 8 x t2) - t2	1 x t2	—
t9	Gate Driver Clock positive edge	1 x t1	1 x t1	1 x t1
t10	Gate Driver Clock negative edge	3 x t1	3 x t1	3 x t1
t11	Gate Driver Clock High Time	((Line Start + Line Begin + Line Data Length) ÷ 8 x t2) + t10	1 x t2	_
t12	Gate Driver Clock Low Time	(Line End Length ÷ 8 x t2) - t10	1 x t2	—



Source Driver Display Timing 3: 4 Pixel per Clock Edge Output (Double Data Rate)

Figure 6-11: Source Driver Display Timing for 4 Pixel per Clock Edge Output

Timing	Description	Value	Min	Мах
t1	Dual Pixel Clock Period	From Pixel Clock Divide	12ns	—
t2	SDCLK Period for 8 Pixel per clock	4 x t1	48ns	—
t3	Line Start Length	(Line Start Length ÷ 8 x t2) + t1	3 x t1	—
t4	Source Driver Latch Enable High time	t3 - (2 x t1)	t3 - (2 x t1)	t <mark>3 - (</mark> 2 x t1)
t5	SDLE deassert to First Data output	(Line Begin Length ÷ 8 x t2)	0	_
t6	Source Driver Output Enable before Data Valid	t2 + t1	t2 + t1	t2 + t1
t7	Data Output Time	Line Data Length ÷ 8 x t2	2 x t2	F
t8	SDOE deassert time from last data output	(Line End Length ÷ 8 x t2) - t2	<mark>1 x</mark> t2	—
t9	Gate Driver Clock positive edge	1 x t1	1 x t1	1 x t1
t10	Gate Driver Clock negative edge	2 x t1	2 x t1	2 x t1
t11	Gate Driver Clock High Time	((Line Start + Line Begin + Line Data Length) ÷ 8 x t2) + t10	1 x t2	—
t12	Gate Driver Clock Low Time	(Line End Length ÷ 8 x t2) - t10	1 x t2	—
t13	SDOEX assert Delay	((REG[030€h] bit <mark>s</mark> 7-3) x t2)	1 x t2	—
t14	SDOEX Pulse Width	1 x t2	1 x t2	1 x t2
t15	SDOED assert Delay	((REG[030Eh] bits 15-11) x t2)	1 x t2	—
t16	SDOED Pulse Width	1 x t2	1 x t2	1 x t2
t17	Data Output Setup Time to SDCLK Edge	1 x t1	1 x t1	1 x t1
t18	Data Output Hold Time to SDCLK Edge	1 x t1	1 x t1	1 x t1

Table 6-11: Source Driver Display Timing for 4 Pixel per Clock Edge Output

6.5.3 Interpreted Gate Driver Timings



The following figure shows an example Gate Driver connection using a Sharp LH1692.

Figure 6-12: Gate Driver Connection Example using Sharp LH1692

Gate driver timings are separated into 2 sections:

- GDCLK: GDCLK is generated from Line Clock (LCLK) and Pixel Data Enable (PDEN). GDCLK is used by the gate drivers to enable gate data output.
- GDSP: GDSP is generated from GDCLK to signal a start pulse.

Gate Driver Display Timings



Figure 6-13: Gate Driver Timing Generation

Timing	Description	Value	Min	Max
t1	GDCLK High Level	Line Start + Line Begin + Line Data Length	4 x DClk	_
t2	GDCLK Low Level	Line End Length	4 x DClk	
t3	1 Line Width	t1 + t2	~	
t4	Frame Sync Length	Frame Sync Length x t3	2 x t3	_
t5	Frame Begin Length	Frame Begin Length x t3	0	_
t6	Gate Driver's Actual output Valid	Fixed Timing	1 x t3	1 x t3
t7	GDCLK to GDSP negative edge	t1 ÷ 2	t1 ÷ 2	t1 ÷ 2
t8	GDCLK to GDSP positive edge\	t1 ÷ 2	t1 ÷ 2	t1 ÷ 2
t9	Frame Data Length	Frame Data Length x t3	1 x t3	_
t10	Frame End Length	Frame End Length x t3	1 x t3	

Table 6-12: Gate Driver Timing Generation

6.6 Power Pin Interface

6.6.1 Power Pin Transition Sequence for PWR[3:0]

The power pins PWR[3:0] operate in a cascade manner with the delay times controlled by register settings (REG[0234h] ~ REG[0238h]).



Figure 6-14: PWR[3:0] Transition Sequence

Symbol	Parameter		Min	Max	Units
tu	Trigger Power up to Power Pin 0 trar	nsition	0	-	ns
0-1 Timing Delay	Power pin 0 to Power pin 1 Timing D	elay		REG[0234h]	Line Clk
1-2 Timing Delay	Power pin 1 to Power pin 2 Timing D	elay	1	REG[0236h]	Line Clk
2-3 Timing Delay	Power pin 2 to Power pin 3 Timing D	elay	1	REG[0238h]	Line Clk

6.6.2 Power Pin Transition Sequence for PWRCOM

The power pin PWRCOM defines the common power control. PWRCOM operations are controlled by the Display Engine update operation as shown in the following figure.



Figure 6-15: PWRCOM Transition Sequence

Table 6-14:	PWRCOM	Transition	Timing
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Symbol	Parameter	Min	Max	Units
t1	PWRCOM Active to Frame Clk	0		ns
t2	Frame Clk to PWRCOM Inactive	0	_	ns

Chapter 7 Clocks

7.1 Clock Descriptions



Chapter 8 Power Management

8.1 Power Management State Description

The S1D13521 controller has the following power states:

- OFF State: Power for the S1D13521 and external SDRAM is off.
- Run State: Normal Operation for the S1D13521. The display can be updated.
- Standby State: S1D13521 is in power save mode and SDRAM is in a Self Refresh state.
- Sleep Mode: S1D13521 is in power save mode and SDRAM is in Self Refresh state. Initiates the Power Pins power down cycles.

The following table summarizes the S1D13521 controller and SDRAM states.

Table 8-1: S1D13521 Controller and SDRAM States

Power Mode	S1D13521 Controller State	S1D13521 PLL State	SDRAM State	SDRAM Data Retained
OFF	Unknown	Unknown	Un <mark>kn</mark> own	No
Run	Active All clocks active	Active	Normal Operation with Auto Refresh	Yes
Standby	Power Save Mode All module clocks gated off PLL is running	Active	Self Refresh	Yes
Sleep	Power Save Mode Power Pin cycle off PLL off	Powered-Down	Self Refresh	Yes

Table 8-2: State Transition Requirements

	Next State Requirements				
Current State	OFF	Run	Standby	Sleep	
OFF	NA	1. Reset 2. Init PLL (Wait 200µs) 3. Init SDRAM (Wait 100µs) 4. Ready for operation	Not Possible. Must Reset to Run State	Not Possible. Must Reset to Run State	
Run	1. Host Save Memory Contents 2. Turn off Power	NA	1. Issue Standby	1. Host Issue Run 2. SDRAM Self Refresh 3. Issue Sleep 4. Power-Pin seq 5. Turn off PLL	
Standby	1. Host issue Run 2. Host Save Memory Contents 3. Turn off Power	 Issue Run SDRAM exit Self Refresh Ready for Operation 	NA	1. Issue Run 2. Issue Sleep 3. Power-Pin Seq 5. Turn Off PLL	
Sleep	1. Turn off Power	1. Issue Run 2. Init PLL (Wait 200µs) 3. SDRAM exit Self Refresh 4. Power-Pin Seq 5. Ready for Operation	1. Host Issue Run 2. Power-Pin Seq 3. Issue standby	NA	



Transitioning to any Power State is only possible from the RUN state.

Figure 8-1: State Transition Diagram

Chapter 9 Host Interface

9.1 Host Cycle Sequences

9.1.1 Command and Parameter Cycle

A typical cycle consists of a Command and a variable number of parameters depending on the expected parameter count for each specific command. The following figures shows a typical cycle.

Host Cycle — Command X Parameters 1 X Parameters 2	<u>}</u>
HRDY	

Figure 9-1: Command Mode Host Cycle Example

The HRDY line is deasserted (low) within 5ns after the last parameter. When the sequencer is ready to accept new commands, HRDY is asserted (high) again.

9.1.2 Memory Access Combination Cycle

Commands that require Host memory access require a combination of Command/Parameter and Register Read/Write cycles. The HRDY line will deassert (low) during the memory read/write data cycles.

Host Cycle —	
HRDY	<u> </u>

0	111	ro	0	2.	M	om	222	· A	co	00	c I	Co	ml	ni	nat	ion	C	wel	6
۲	n	16	1	-2.	111	eme	<i>//</i>)		ιιι	es	D	$-\upsilon$	m	u	nui	i O I		yci	e

EPSON

9.2 HRDY (Wait Line) Usage

When a command is issued, the command sequencer must execute a set of instruction codes based on the specific command. The execution time required for each command depends on the number of instruction codes that must be completed.

Once a command is issued, the host interface must not issue any new commands until HRDY is asserted High. If the HRDY line is not used, the Host can poll the Sequence Controller Busy Status bit in REG[000Ah] using the RD_REG command.

Note

RD_REG is implemented outside of the Sequence Controller and is specifically designed to allow execution in parallel with other command sequences. This is useful for polling the Sequence Controller Busy Status by Hosts that do not have HRDY.

The following figure shows a typical command/parameter sequence using Sequence Controller Busy Status polling.

Host Cycle — Command Param 1 Param 2 Param N RD_REC	G (000A (Sys Register Address	s Stat) Sys Stat Sequence Controller Busy	Sequence Controller Not Busy	
Figure 9-3: Command Mode Host Cycle Exa	mple for H	lost without	HRDY	

9.3 Command Operation



The following figure shows a typical command mode operation with parameter/data writes only.

Figure 9-4: Command Mode Operation - Parameter/Data Writes Only

The following figure shows a typical command mode operation for reading register data.



9.4 Command List

The following commands are applicable for the 16-bit Indirect Interface.

Code							
16-bit Indirect - 2 bytes	Command	1	2	3	4	5	Description
			System Co	mmands			
0x00	INIT_CMD_SET	SPI Config	SFM Adr[15:0]	SFM[23:16]	_	—	Initialize Instruction code from Specific Serial Flash Address
0x01	INIT_PLL_STBY	PLL Config0	PLL Config1	PLL Config2	—	—	Initialize PLL and Go Into Standby Mode
0x02	RUN_SYS	_	_	_	_	_	Run System using PLL
0x04	STBY	—	—	—	—	—	Go to Standby Mode
0x05	SLP	—	—	—	—	—	Go to Sleep Mode
0x06	INIT_SYS_RUN	—	—	—	—	—	Initialize System and Go into Run State
0x07	INIT_SYS_STBY	—	—	—	—	—	Initialize System and Go into Standby State
0x08	INIT_SDRAM	SDRAMCFG0	SDRAMCFG1	SDRAMCFG2	SDRAMCFG3		Initialize SDRAM
0x09	INIT_DSPE_CFG	HSIZE	VSIZE	SDRVCFG	GDRVCFG	LUT Index Format CFG	Initialize Display Engine
0x0A	INIT_DSPE_TMG	Frame Sync CFG	Frame Begin/End CFG	Line Sync CFG	Line Begin/End CFG	Pixel Clock CFG	Initialize Driver Timings
0x0B	INIT_ROTMODE	ROTMODE	—	—	—	—	Initialize Rotation Mode Timings
		Regis	ter and Memory	Access Comma	ands		
0x10	RD_REG	REGADDR[15 :0]	RDATA[15:0]	—	_	—	Read Register Refer to detailed descriptions
0x11	WR_REG	REGADDR[15 :0]	WDATA[15:0]	_	_	_	Write Register Refer to detailed descriptions
0x12	RD_SFM	_	_	_	_	_	Trigger Serial Flash Read Operation
0x13	WR_SFM	WDATA[15:0]	—	—	—	—	Trigger Serial Flash Write Operation
0x14	END_SFM	_	_	_	_		END SFM Operation
			Burst Access	Commands			
0x1C	BST_RD_SDR	MA[15:0]	MA <mark>[31</mark> :16]	BC[15:0]	BC[31:16]	—	Start Burst Read SDRAM Memory
0x1D	BST_WR_SDR	MA[15:0]	MA[31:16]	BC[15:0]	BC[31:16]	—	Start Burst Write SDRAM Memory
0x1E	BST_END_SDR					_	Burst End
0.00			Image Loading	g Commands	[[
0x20		ARG[15:0]	_	_	_	_	
0x22	LD_IMG_AREA	ARG[15:0]	XSTART[15:0]	YSTART[15:0]	WIDTH[15:0]	HEIGHT[15:0,	parameters
0x23							Load Image End
0x24	LD_IMG_WAIT	_	_				Load Image Wait End
0x25	LD_IMG_SETADR	MA[15:0]	MA[31:16]	—	—	—	Address
0x26	LD_IMG_DSPEADR	—	_	—	—	—	Set Load Image to use Display Engine's Address
			Polling Co	mmands			Wait For Diaplay Engine
0x28	WAIT_DSPE_TRG	—	—	—	—	—	Trigger Done
0x29	WAIT_DSPE_FREND	—	—	_	—	—	Frame End
0x2A	WAIT_DSPE_LUTFREE	_	—	—	—	—	Wait For Display Engine At least 1 LUT is Free
0x2B	WAIT_DSPE_MLUTFREE	LUT Mask [15:0]	—	—	—	—	Wait For Display Engine At least 1 Masked LUT is Free

Code											
16-bit Indirect	16-bit Indirect Command - 2 bytes		2	3	4	5	Description				
- 2 bytes			2	5	-	5					
	Waveform Update Commands										
0x30	RD_WFM_INFO	MA[15:0]	MA[31:16]	—	—	—	Read Waveform Information				
0x32	UPD_INIT	—	—	_	—	—	Update Buffer Initialize				
0x33	UPD_FULL	ARG[15:0]	—	_	—	—	Update Buffer Full				
0x34	UPD_FULL_AREA	ARG[15:0]	XSTART[15:0]	YSTART[15:0]	WIDTH[15:0]	HEIGHT[15:0]	Update Buffer Full Area				
0x35	UPD_PART	ARG[15:0]	—	_	—	—	Update Buffer Partial				
0x36	UPD_PART_AREA	ARG[15:0]	XSTART[15:0]	YSTART[15:0]	WIDTH[15:0]	HEIGHT[15:0]	Update Buffer Partial Area				
0x37	UPD_GDRV_CLR		—			—	Gate Driver Clear Command				
0x38	UPD_SET_IMGADR	ADR[15:0]	ADR[31:16]	—	—	—	Set Image <mark>B</mark> uffer Start Address				
0x38-0x3F	Reserved	_	_	_		_	Reserved				

Table 9-1: Host Interface Command Summary

9.5 Host Interface Command Descriptions

The Command Sequencer supports up to 64 available commands. The first 8 commands (command codes 0x00 ~ 0x07) turn on the temporary clock enable until the command sequence has finished. This feature is for implementing commands (i.e. INIT_CMD_SET, INIT_PLL, SLP) where the S1D13521 is, or will be, in SLP mode before or after the command sequence command is completed. In SLP mode, the input clock is gated off in order to minimize power consumption. However, a clock is needed for the Sequencer Controller logic while it is operating.

Three commands are reserved and cannot be re-programmed.

- 0x00 INIT_CMD_SET
- 0x10 RD_REG
- 0x11 WR_REG

These commands are hard-coded in logic allowing them to operate even before the pre-programmed command sequence is loaded into the chip. RD_REG (which can be executed in parallel with the Sequence Controller) can poll the busy status of the Sequence Controller to determine when the previous command sequence has finished. This is useful for Hosts that have no HRDY support.

Note

Although the RD_REG and WR_REG commands can be executed in parallel with the Sequence Controller, register reads/writes are not recommended while the Sequence Controller is in operation. The exception to this rule is polling the busy status bit.

9.5.1 INIT_CMD_SET (0x00 + 3 parameters)

This command initializes the Command Interface instruction table and codes. The parameters setup the SPI operating mode and the Serial Flash Memory address where the instruction table and codes are stored.

Parameter Count = 3

Parameter 1	Parameter 1 (Recommended Setting = 0x0041)											
	n/a											
15	14	13	12	11	10	9	8					
SPI Flash Access Mode Select	SPI Flash Read Command Select	SPI Flas	h Clock Divide Seled	ct bits 2-0	SPI Flash Clock Phase Select	SPI Flash Clock Polarity Select	SPI Flash Enable					
7	6	5	4	3	2	1	0					

bit 7

SPI Flash Access Mode Select

This bit selects between Display Engine access mode and Host Register access mode. This bit must be set to 1b before performing a Display Engine operation to allow the Display Engine to communicate with SPI Flash Memory.

When this bit = 0b, Host Register access mode is selected.

When this bit = 1b, Display Engine access mode is selected.

bit 6 SPI Flash Read Command Select This bit selects which serial flash command is used for reading data and depends on the SPI Flash Memory device. Refer to the device data sheet to determine the appropriate setting. When this bit = 0b, the serial flash read speed is Low. When this bit = 1b, the serial flash read speed is High. bits 5-3 SPI Flash Clock Divide Select bits [2:0] These bits select the divide ratio for the SPI Flash Clock which is derived from either the PLL output or CLKI depending on the setting of the PLL Bypass Mode Enable bit, REG[0016h] bit 0. For further details on the clock structure, see Section Chapter 7, "Clocks" on page 45.

bits 5-3	SPI Flash Clock Divide Ratio	bits 5-3	SPI Flash Clock Divide Ratio
000b	1:2	100b	1:6
001b	1:3	101b	1:7
010b	1:4	110b	1:8
011b	1:5	_111b	1:9

bit 2 SPI Flash Clock Phase Select

This bit selects the SPI Flash clock phase. For a summary of the SPI Flash Memory clock phase and polarity settings, see Table 10-19 "SPI Flash Clock Phase and Polarity," on page 100.

bit 1 SPI Flash Clock Polarity Select (CPOL)

This bit selects the SPI Flash clock polarity. The following table summarizes the SPI Flash clock polarity and phase settings.

Table 9-3 :	SPI Flash	<mark>Clock Phas</mark> e	and Polarity

bit 2	bit 1	Val <mark>id</mark> Data	Clock Idling Status
Ob	Ob	Rising edge of SPI Flash Clock	Low
du	1b	Falling edge of SPI Flash Clock	High
16	0b	Falling edge of SPI Flash Clock	Low
	1b	Rising edge of SPI Flash Clock	High

bit 0

SPI Flash Enable

This bit controls the SPI Flash Memory interface logic.

When this bit = 0b, the SPI Flash Memory interface is disabled.

When this bit = 1b, the SPI Flash Memory interface is enabled.

Note

The SPI Flash Memory interface should be disabled (REG[0204h] bit 0 = 0b) before programming the SPI Flash registers, REG[0200h] ~ REG[0208h].

Parameter 2							
		Se	erial Flash Memory A	ddress Select bits 15	5-8		
15	14	13	12	11	10	9	8
		S	erial Flash Memory	Address Select bits 7-	-0		
7	6	5	4	3	2	0	0
Parameter 3							
15	14	13	12	11	10	9	8
		Se	rial Flash Memory A	ddress Select bits 23	-16		
7	6	5	4	3	2	0	0

Parameter 3 bits 7-0 Parameter 2 bits 15-0

Serial Flash Memory Address Select bits [23:0]

These bits specify the memory start address in the Serial Flash Memory where the Instruction Codes are located.

9.5.2 INIT_PLL_STBY (0x01 + 3 parameters)

This command initializes the PLL and sets the S1D13521 into Standby Mode. PLL Configuration is programmed using the three input parameters. When PLL Lock is asserted, this command sequence is completed.

Functions performed:

- 1. Program PLL registers
- 2. Disable PLL Power Down (REG[0016h]) to 0001h
- 3. Wait for PLL Lock
- 4. Program State Status register to Standby Mode (REG[000Ah] bits 12-10 = 2h)
- 5. Turn On Power Save Mode (REG[0006h] bit 0 = 1b)

Next Command Blocking: Yes

Parameter 1							
			PLL Settir	ng 0 bit <mark>s</mark> 7-0			
15	14	13	12	11	10	9	8
n	/a			M-Divide	er bits 5-0		
7	6	5	4	3	2	1	0

bits 15-8

PLL Setting 0 bits [7:0]

These bits must be set to F8h.

bits 5-0

M-Divider bits [5:0]

These bits determine the divide ratio between CLKI and the actual input clock to the PLL. These bits must be set such that the internal input clock to the PLL (PLLCLK) is between 1MHz and 2MHz.

	M-Divider Ratio	bits 5-0
	1:1	0h
	2:1	01h
T 🔥 🖉	3:1	02h
T	4:1	03h
T 🗙 🔪	•	•
	•	•
	•	•
	33:1	20h
	Reserved	21h to 3Fh

Table 9-4: PLL M-Divide Selection

Parameter 2					U			
			PLL Setting	g 1 bits 15-8				
15	14	13	12	11		10	9	8
	PLL Setting 1 bits 7-0							
7	6	5	4	3		2	1	0

bits 15-0

PLL Setting 1 bits [15:0] These bits must be set to 2880h.

Parameter 3							
n/a				L-Counter bits 6-0)		
15	14	13	12	11	10	9	8
			PLL Set	ting 2 bits 7-0	•		
7	6	5	4	3	2	1	0
bits 14-8	L-C	Counter bits [6	5:01				

These bits are used to configure the PLL Output (in MHz) and must be set according to the following formula.

PLL Output = (L-Counter + 1) x PLLCLK = LL x PLLCLK

Where:

PLL Output is the desired PLL output frequency (in MH L-Counter is the value of this register (in decimal). PLLCLK is the internal input clock to the PLL (in MI

Table 9-5 PLL Setting B	Ix <mark>a</mark>	mp	le
-------------------------	-------------------	----	----

Target Frequency (MHz)	LL	CLKI Input Clock (MHz)	M-Divider (bits 5-0	M-Divide Ratio	PLLCLK (MHz)	POUT (MHz)
133	110	12	09h	10:1	1.2	132

bits 7-0

PLL Setting 2 bits [7:0

These bits must be set to 00h.

9.5.3 RUN_SYS (0x02 + 0 parameters)

This command places the S1D13521 into normal operation mode. This includes enabling the PLL and/or disabling power save mode (i.e. removing the S1D13521 from Standby or Sleep mode).

Functions performed:

- 1. Disable PLL Power Down (if not disabled already)
- 2. Wait for PLL Lock (if step 1 is valid)
- 3. Disable Power Save Mode (REG[0006h] bit $0 \le 0$)
- 4. Trigger Power Pin On Sequence
- 5. Trigger SDRAM Exit Self-Refresh
- 6. Wait for SDRAM Ensure Self-Refresh is exited and Power Pin sequence is done
- 7. Program State Status Register (REG[000Ah] bits 12-10 to 1h (Normal Operation)

Next Command Blocking: Yes

9.5.4 STBY (0x04 + 0 parameters)

This command places the S1D13521 into Standby mode. To wake up from Standby mode, use the RUN_SYS command.

Functions performed:

- 1. Wait for all modules to be idle (HMEM, I2C, SPI, PWR, 3-wire, SDRAM, and DSPE)
- 2. Power Pin (Enter Off State)
- 3. SDRAM (Enter Self-Refresh Mode)
- 4. SDRAM (Wait for Self-Refresh Mode Entered) and Power Pin (Wait for Off State Entered)
- 5. Program State Status register to Standby Mode (REG[000Ah] bits 12-10 = 2h)
- 6. Power Save (Enable)

Next Command Blocking: Yes

9.5.5 SLP (0x05 + 0 parameters)

This command places the S1D13521 into Sleep mode. Sleep mode differs from Standby mode in that the PLL is powered down. To wake up from Sleep mode, use the RUN_SYS command.

Functions performed:

- 1. Wait for all modules to be idle (HMEM, I2C, SPI, PWR, 3-wire, SDRAM, and DSPE)
- 2. Power Pin (Enter Off State)
- 3. SDRAM (Enter Self-Refresh Mode)
- 4. SDRAM (Wait for Self-Refresh Mode Entered)
- 5. Power Pin (Wait for Off State Entered)
- 6. Power Save (Enable)
- 7. PLL Power Down (Enable Power Down)

Next Command Blocking: Yes

9.5.6 INIT_SYS_RUN (0x06 + 0 parameters)

This command initializes the S1D13521 according to the requirements of the customer.

Functions performed:

- 1. Configure PLL (PLLM = 3
- 2. PLL RUN
- 3. PLL (Wait Lock)
- 4. Disable Power Save Mode
- 5. **SDRAM** Init (according to customer setting)
- 6. DSPE Init (according to customer setting)
- 7. PWRPIN Init
- 8. Wait SDRAM Init done and PWRPIN POWER-ON
- 9. Power State (Write 0x1)

Next Command Blocking: Yes

9.5.7 INIT_SYS_STBY (0x07 + 0 parameters)

This command initializes the S1D13521 according to the requirements of the customer and places the S1D13521 into Standby mode.

Functions performed:

- 1. Configure PLL (PLLM = 3
- 2. PLL RUN
- 3. PLL (Wait Lock)
- 4. Disable Power Save Mode
- 5. SDRAM Init (according to customer setting)
- 6. DSPE Init (according to customer Setting)
- 7. PWRPIN Init
- 8. SDRAM Enter Self Refresh Mode, Power-Pin Off State
- 9. Power State (Write 0x2)
- 10. Enter Power Save Mode.

Next Command Blocking: Yes

9.5.8 INIT_SDRAM (0x08 + 4 parameters)

This command initializes the SDRAM.

Functions performed:

- 1. Setup the SDRAM registers using the specified parameters
- 2. Initialize the SDRAM
- 3. Wait for the SDRAM Initialize to complete

Next Command Blocking: Yes

Parameter 1							
SDRAM Power Down Disable	SDRAM	Refresh Cycle Time	e bits 1-0	SDRAM Refres	sh Rate bits 1-0	SDRAM Row Ac	tive Time bits 1-0
15	14	13	12	11	10	9	8
16-bit SDRAM Enable	SDRAM tRP Latency Select	SDRAM tRCD Latency Select	SDRAM tCL Latency Select	n/a	SDRAM Colum bits	n Address Count 1-0	SDRAM Burst Type Select
7	6	5	4	3	2	1	0

bit 15



- SDRAM Power Down Disable
- This bit controls the SDRAM power down function which dynamically disables the SDRAM clock when the SDRAM is idle.
- When this bit = 0b, the SDRAM power down function is enabled.
- When this bit = 1b, the SDRAM power down function is disabled.

SDRAM Refresh Cycle Time bits [2:0]

These bits specify the SDRAM Refresh Cycle Time (tRFC) using the following formula. Refresh cycle time = REG[0100h] bits 14-12 + 4

bits 11-10SDRAM Refresh Rate bits [1:0]These bits specify the SDRAM refresh rate for 8192 rows.

REG[0100h] bits 11-10	Refresh Rate
00b	64 ms
01b	128 ms
10b	256 ms
11b	512 ms

Table 9-6 : SDRAM Refresh Rate Selection

bits 9-8 SDRAM Row Active Time bits [1:0]

These bits specify the Row Active Time (tRAS) which defines the minimum time for an opened row to be issued a precharge.

tive Time (tRA	(S) Selection
	uve i une (una

REG[0100h] bits 9-8	Row Active Time
00b	5 clocks
01b	6 clocks
10b	7 clocks
11b	8 <mark>cloc</mark> ks

16-bit SDRAM Enable
This bit specifies whether 16 or 32-bit SDRAM is selected.
When this bit = 0b, 32-bit SDRAM mode is selected.
When this bit = 1b, 16-bit SDRAM mode is selected.
SDP AM (PP Latency Select
This bit selects the Row Precharge Time which is the precharge time required before a row
can be activated again.
When this bit = 0b, the row precharge time is 2 clocks .
When this bit $= 1b$, the row precharge time is 3 clocks.
SDRAM tRCD Latency Select
This hit selects the Dow to Column Latency
This bit selects the Row to Column Latency.
When this bit = 0b, the row to column latency is 2 clocks.
When this bit = 1b, the row to column latency is 3 clocks.
SDRAM tCL Latency Select
This bit selects the Column Read to Data Available Latency.
When this bit = 0b, the column read to data available latency is 2 clocks
When this bit $= 1b$, the column read to data available latency is 2 clocks.
when this bit – 10, the column read to data available fatchey is 5 clocks.

bits 2-1 SDRAM Column Address Count bits [1:0] This bit specifies the number of column addresses used for the SDRAM.

REG[0100h] bits 2-1	Column Address Count
00b	256
01b	512
10b	1024
11b	2048

Table 9-8: SDRAM Column Address Count Selection

bit 0

SDRAM Burst Type Select

This bit selects the type of burst used for SDRAM accesses. When this bit = 0b, full page burst is selected. This setting is used for standard SDRAM. When this bit = 1b, fixed 8-burst is selected. This setting is used for mobile SDRAM.

Parameter 2										
SDRAM Refresh Clock Divide Select bits 15-8										
15	14	13	12	11	10	9	8			
	SDRAM Refresh Clock Divide Select bits 7-0									
7	6	5	4	3	2	0	0			

bits 15-0

SDRAM Refresh Clock Divide Select bits [15:0]

These bits select the divide used to determine the SDRAM Refresh Clock frequency. These bits should be set such that the resulting refresh clock is approximately 64KHz. For further information on the clock structure, see Section Chapter 7, "Clocks" on page 45. Refresh Clock Divide = REG[0106h] bits 15-0 + 1

The refresh clock is calculated using the following formula. Refresh clock frequency = CLKI frequency + Refresh Clock Divide

For example, the default register value of 02EDh results in the following refresh frequency when CLKI is 24MHz.

Refresh clock freque	ency = <mark>2</mark> 4N	MHz ÷ 375
	-64k	KHz

Parameter 5							
n/a							
15	14	13	12	11	10	9	8
n/a		0	0	1	n/a		
7	6	5	4	3	2	1	0

Parameter 3 must be set to 08h.

Parameter 4							
n/a	SDRAM Driver Strength bits 1-0 Temperature Compensated Self Refresh bits 1-0 Partial Array Self Refresh						pits 2-0
15	14	13	12	11	10	8	
n/a					SDRAM S	ize bits 1-0	Extended Mode Register Program on Initialization Enable
7	6	5	4	3	2	1	0

bits 14-13

SDRAM Driver Strength bits [1:0]

These bits only have an effect when the Extended Mode Register Program On Initialization Enable bit is set to 1b, REG[010Ah] bit 0 = 1b. These bits set the value for Driver Strength (DS) that is programmed into the extended mode register of the mobile SDRAM.

 Table 9-9 :
 SDRAM Driver Strength Selection

	bits 14-13	Driver Strength	
	00b	Full Strength	
	01b	Half Strength	
	10b	Quarter Strength	
	11b	Eighth Strength	
bits 12-11	Temperature Compensated Self These bits only have an effect of tion Enable bit is set to 1b, REC refresh rate to be varied based of for Temperature Compensated mode register of the mobile SE	f Refresh bits [1:0] when the Extended Mode Ro G[010Ah] bit 0 = 1b. Mobile on the temperature of the SE Self Refresh (TCSR) that is DRAM.	egister Program On Initializa- e SDRAM allows the self DRAM. These bits set the value programmed into the extended
bits 10-8	Partial Array Self Refresh bits These bits only have an effect tion Enable bit is set to 1b, RE Array Self Refresh (PASR) tha mobile SDRAM.	[2:0] when the Extended Mode Ro G[010Ah] bit $0 = 1b$. These t is programmed into the ext	egister Program On Initializa- bits set the value for Partial tended mode register of the
bits 2-1	SDRAM Size bits [1:0] These bits specify the SDRAM placement.	size, in M bytes. This settin	ng is used for bank address

bits 2-1	SDRAM Size
00b	8M bytes
01b	16M bytes
10b	32M bytes
11b	64M bytes

 Gable 9-10 :
 SDRAM Size Selection

Extended Mode Register Program On Initialization Enable
When mobile SDRAM is used, this bit controls whether the extended mode register is programmed when the SDRAM is initialized, REG[0102h] bit 0 = 1b.
When this bit = 0b, the extended mode register is not programmed when the SDRAM is initialized.
When this bit = 1b, the extended mode register is programmed when the SDRAM is initialized.

9.5.9 INIT_DSPE_CFG (0x09 + 5 parameters)

This command initializes the Display Engine.

Functions performed:

bit 0

1. Initializes the Display Engine according to the specified parameters

2. Set REG[032Ch] to 0x0400, Area Size Mode Enabled

Denometer 4								
Parameter 1								
			Panel HSiz	ze bits 15-8				
15	14	13	12	11	10	9	8	
			Panel HSi	ze bits 7-0				
7	6	5	4	3	2	1	0	
Devenuetor 2					<u> </u>			
Parameter 2								
			Panel VSiz	ze bits 15-8				
15	14	13	12	11	10	9	8	
			Panel VSi	Size bits 7-0				
7	6	5	4	3	2	1	0	
Denem ster 0								
Parameter 3				·				
	Osuma Daiusa Ohia			Source Driver	Source Driver	Source Driver	Source Driver	
	Source Driver Chip	Enable Start bits 3-0		Count Select	Reverse	Output Reverse	Shift Right	
15	14	13	12	11	10	9	8	
	•	•	Source Driver Outpu	t Size Select bits 7-0	0	•	•	
7	6	5	4	3	2	1	0	
Parameter 4								
						Source Driver	Source Driver	
		n	/a			Swap Padding	Early SDOE	
45		40	40		10	FIXEIS	Asselt Disable	
15	14	13	12	11	10	9 Gate Driver	o Gate Driver Start	
		n	/a			Right/Left Select	Pulse Polarity	
7	6	5	4	3	2	1	0	
Parameter 5								
Display Engine								
Software Reset				n/a				
(000)		10			1 10			
15	14	13	12	11	10	9	8	
Enable		n	/a		LUT li	ndex Format Select b	bits 2-0	
7	6	5	4	3	2	1	0	

9.5.10 INIT_DSPE_TMG (0x0A + 5 parameters)

This command initializes the display timing information.

Functions performed:

1. Initialize the Display Engine display timing according to parameters 1-4

2. Initialize the Pixel Clock according to parameter 5

Parameter 7	1						
			n	/a			
15	14	13	12	11	10	9	8
			Frame Sync L	ength bits 7-0			
7	6	5	4	3	2	1	0
Paramotor '	2						
i arameter z	L						
		1	Frame End L	ength bits 7-0	1		
15	14	13	12	11	10	9	8
		1	Frame Begin I	Length bits 7-0	1		
7	6	5	4	3	2	1	0
Denemater	0						
Parameter	3			•			
			n	/a			
15	14	13	12	11	10	9	8
			Line Sync Le	ength bits 7-0			
7	6	5	4	3	2	1	0
				<u> </u>	<u> </u>		
Parameter 4	4				•		
			Line End Le	ngth bits 7-0			
15	14	13	12	11	10	9	8
			Line Begin L	ength bits 7-0			
7	6	5	4	3	2	1	0
	•					•	•
Parameter	5	<u> </u>					
			n	/a			
15	14	13	12	11	10	9	8
	n/a		Pixel Clock Bypass Enable		Pixel Clock Divid	le Select bits 3-0	
7	6	5	4	3	2	1	0
	_			_			

9.5.11 INIT_ROTMODE (0x0B + 1 parameter)

This command initializes the S1D13521 Rotation Mode

Functions performed:

1. Set REG[032Ch] bits 9-8 with the specified Rotation Mode

2. Set REG[0140h] bits 9-8 with the specified Rotation Mode

Parameter 1									
n/a Rotation Mode bits 1-0						ode bits 1-0			
15	14	13	12	11	10	9	8		
	n/a								
7	6	5	4	3	2	1	0		

9.5.12 RD_REG (0x10 + 2 parameters)

This command initiates a low level register read from the address specified by parameter 1. The returned data value is available in parameter 2.

Parameter 1							
			Register Ad	dress bits 15-8			
15	14	13	12	11	10	9	8
			Register Ad	dress bits 7-0			
7	6	5	4	3	2	1	0
		•				_	
Parameter 2							
			Register Rea	d Data bits 15-8			
15	14	13	12	11	10	9	8
		•	Register Rea	d Data bits 7-0			
7	6	5	4	3	2	1	0

9.5.13 WR_REG (0x11 + 2 parameters)

This command initiates a low level register write of the data specified by parameter 2 to the address specified by parameter 1..

Parameter 1	arameter 1									
			Register Ade	dress bits 15-8						
15	14	13	12	11	10	9	8			
			Register Ad	dress bits 7-0						
7	6	5	4	3	2	1	0			
Parameter 2			<							
			Register Write	e Data bits 15-8						
15	14	13	12	11	10	9	8			
	Register Write Data bits 7-0									
7	6	5	4	3	2	1	0			

9.5.14 RD_SFM (0x12 + 0 parameters)

This command initiates a low level read from the Serial Flash Memory.

9.5.15 WR_SFM (0x13 + 1 parameter)

This command initiates low level write of the data specified by parameter 1 to the Serial Flash Memory.

Parameter 1									
15	14	13	12	11	10	9	8		
Serial Flash Memory Write Data bits 7-0									
7	6	5	4	3	2	1	0		

9.5.16 END_SFM (0x14 + 0 parameters)

This command ends a low level operation to/from the Serial Flash Memory.

9.5.17 BST_RD_SDR (0x1C + 4 parameters)

This command starts a memory burst read operation.

Functions performed:

- 1. End Previous Host Memory access operation if currently active.
- 2. Setup Read Mode and Raw Access Mode on REG[0140h]
- 3. Setup Raw Address
- 4. Setup Burst Size
- 5. Trigger Start and Wait for Ready..

Memory Address bits 15-8 15 14 13 12 11 10 9 Memory Address bits 7-0 7 6 5 4 3 2 1 Parameter 2 Memory Address bits 31-24	8
15 14 13 12 11 10 9 Memory Address bits 7-0 7 6 5 4 3 2 1 Parameter 2 Memory Address bits 31-24	8
Memory Address bits 7-0 7 6 5 4 3 2 1 Parameter 2 Memory Address bits 31-24 Memory Address bits 31-24	0
7 6 5 4 3 2 1 Parameter 2 Memory Address bits 31-24 Memory Address bits 31-24 Memory Address bits 31-24 Memory Address bits 31-24	0
Parameter 2 Memory Address bits 31-24	•
Parameter 2 Memory Address bits 31-24	
Memory Address bits 31-24	
15 14 13 12 11 10 9	8
Memory Address bits 23-16	
7 6 5 4 3 2 1	0
Parameter 3	
Burst Size bits 15-8	
15 14 13 12 11 10 9	8
Burst Size bits 7-0	
7 6 5 4 3 2 1	0
Parameter 4	
Burst Size bits 31-24	
15 14 13 12 11 10 9	8
Burst Size bits 23-16	
7 6 5 4 3 2 1	0

j?

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9.5.18 BST_WR_SDR (0x1D + 4 parameters)

This command starts a memory burst write operation.

Functions performed:

- 1. End Previous Host Memory access operation if currently active.
- 2. Setup Write Mode and Raw Access Mode on REG[0140h]
- 3. Setup Raw Address
- 4. Setup Burst Size
- 5. Trigger Start and Wait for Ready....

Parameter 1							
			Memory Add	ress bits 15-8			
15	14	13	12	11	10	9	8
		•	Memory Ade	dress bits 7-0		•	
7	6	5	4	3	2	1	0
Parameter 2							
			Memory Add	ess bits 31-24			
15	14	13	12	11	10	9	8
			Memory Add	ess bits 23-16		•	
7	6	5	4	3	2	1	0
Parameter 3							
			Burst Siz	e bits 15-8			
15	14	13	12	11	10	9	8
			Burst Siz	e bits 7-0			
7	6	5	4	3	2	1	0
Parameter 4							
			Burst Size	e bits 31-24			
15	14	13	12	11	10	9	8
			Burst Size	e bits 23-16			
7	6	5	4	3	2	1	0

9.5.19 BST_END_SDR (0x1E + 0 parameters)

This command terminates a burst operation before it has completed.

Functions performed:

1. End Previous Host Memory access operation if currently active

2. Wait for Busy to end

9.5.20 LD_IMG (0x20 + 1 parameter)

This command starts a Full Frame Memory Load operation according to the data packing settings in parameter 1.

Functions performed:

- 1. End Previous Host Memory access operation if currently active.
- 2. Setup Write Mode and Packed Access Mode on REG[0140h]
- 3. Setup Packing Bpp Select using Parameter
- 4. Setup Full Display Size Update (Copy size from Display Engine's registers)
- 5. Trigger start transfer.

Parameter 1							
			n	/a			
15	14	13	12	11	10	9	8
r	/a	Data Packing	Select bits 1-0	n/a			
7	6	5	4	3	2	1	0

9.5.21 LD_IMG_AREA (0x22 + 5 parameters)

This command starts an Area Defined Frame Memory Load operation according to the data packing settings in the parameters.

Functions performed:

- 1. End Previous Host Memory access operation if currently active.
- 2. Setup Write Mode and Packed Access Mode on REG[0140h]
- 3. Setup Packing Bpp Select using Parameter
- 4. Setup Size with Parameters.
- 5. Trigger start transfer

Parameter 1							
			r	n/a			
15	14	13	12	11	10	9	8
r	n/a	Data Packing	Select bits 1-0		n	/a	
7	6	5	4	3	2	1	0
		•		•			
Parameter 2	2						
	n/a			Packed Pivel R	ectangular X-Start P	Osition hits 12-8	

	n/a			Packed Pixel R	ectangular X-Start P	osition bits 12-8				
15	14	13	12	11	10	9	8			
Packed Pixel Rectangular X-Start Position bits 7-0										
7	6	5	4	3	2	0	0			

Parameter 3										
	n/a		Packed Pixel Rectangular Y-Start Position bits 12-8							
15	14	13	12	11	10	9	8			
Packed Pixel Rectangular Y-Start Position bits 7-0										
7	6	5	4	3	2	0	0			

Parameter 4	4									
	n/a			Packed Pixel Rectangular Width bits 12-8						
15	14	13	12	11	10	9	8			
			Packed Pixel Recta	angular Width bits 7-0)					
7	6	5	4	3	2	0	0			
Parameter :	5									
	n/a			Packed Pi	xel Rectangular Heig	ht bits 12-8				
15	14	13	12	11	10	9	8			

Packed Pixel Rectangular Height bits 7-0

4

3

2

0

0

9.5.22 LD_IMG_END (0x23 + 0 parameters)

6

This command terminates a Load Image operation before it has completed and waits for the image load to finish before writing to the Memory.

Functions performed:

7

1. End Previous Host Memory access operation if currently active.

5

2. Wait for Busy to end

9.5.23 LD_IMG_WAIT (0x24 + 0 parameters)

This command waits for a Load Image operation to finish writing to the memory.

Functions performed:

1. Wait for REG[0140h] bit 12 - wait for busy to deassert.

9.5.24 LD_IMG_SETADR (0x25 + 2 parameters)

This command loads an image to the address specified by the Host (see REG[0144h] ~ REG[0146h]).

9.5.25 LD_IMG_DSPEADR (0x26 + 0 parameters)

This command loads an image to the address specified by the Display Engine image buffer (see REG[0310h] ~ REG[0312h]).

9.5.26 WAIT_DSPE_TRG (0x28 + 0 parameters)

This command waits for the Display Engine operation to complete.

Functions performed: 1. Wait for REG[0338h] bit 0 to return 0b

9.5.27 WAIT_DSPE_FREND (0x29 + 0 parameters)

This command wait for the Display Engine to complete outputting display frames.

Functions performed: 1. Wait for REG[0338h] bit 3 to return 0b

9.5.28 WAIT_DSPE_LUTFREE (0x2A + 0 parameters)

This command wait for the Display Engine to have at least one free LUT.

Functions performed: 1. Wait for REG[0338h] bit 6 to return 1b

9.5.29 WAIT_DSPE_MLUTFREE (0x2B + 1 parameter)

This command waits for the Display Engine to have at least one free Masked LUT.

Functions performed:

1. Setup LUT Mask register with parameter 1

2. Wait for REG[0338h] bit 7 to return 1b

Parameter 1										
			LUT Mask	Setting 15:8						
15	14	13	12	11	10	9	8			
	LUT Mask Setting 7:0									
7	6	5	4	3	2	1	0			

9.5.30 RD_WFM_INFO (0x30 + 2 parameters)

This command issues a Waveform Read operation to the Display Engine.

Functions performed:

- 1. Setup Waveform Address
- 2. Trigger Waveform Read operation
- 3. Wait for Trigger completed

Waveform Header Serial Flash Address bits 15-8 15 14 13 12 11 10 9 8 Waveform Header Serial Flash Address bits 7-0 7 6 5 4 3 2 1 0 Naveform Header Serial Flash Address bits 7-0 7 6 5 4 3 2 1 0 Parameter 2 n/a 15 14 13 12 11 10 9 8 Waveform Header Serial Flash Address bits 23-16	Parameter 1					•							
15 14 13 12 11 10 9 8 Waveform Header Serial Flash Address bits 7-0 7 6 5 4 3 2 1 0 Parameter 2 n/a 15 14 13 12 11 10 9 8 Waveform Header Serial Flash Address bits 23-16			Wa	veform Header Seria	I Flash Address bits	s 15-8							
Waveform Header Serial Flash Address bits 7-0 7 6 5 4 3 2 1 0 Parameter 2 n/a 15 14 13 12 11 10 9 8 Waveform Header Serial Flash Address bits 23-16	15	14	13	12	11	10	9	8					
7 6 5 4 3 2 1 0 Parameter 2 n/a 15 14 13 12 11 10 9 8 Waveform Header Serial Flash Address bits 23-16		Waveform Header Serial Flash Address bits 7-0											
Parameter 2 n/a 15 14 13 12 11 10 9 8 Waveform Header Serial Flash Address bits 23-16	7	6	5	4	3	2	1	0					
Parameter 2 n/a 15 14 13 12 11 10 9 8 Waveform Header Serial Flash Address bits 23-16													
n/a 15 14 13 12 11 10 9 8 Waveform Header Serial Flash Address bits 23-16	Parameter 2	Parameter 2											
15 14 13 12 11 10 9 8 Waveform Header Serial Flash Address bits 23-16				n	/a								
Waveform Header Serial Flash Address bits 23-16	15	14	13	12	11	10	9	8					
	Waveform Header Serial Flash Address bits 23-16												
7 6 5 4 3 2 1 0	7	6	5	4	3	2	1	0					

9.5.31 UPD_INIT (0x32 + 0 parameters)

This command issues an Update Buffer Refresh with data from the Image Buffer. No display operation will occur.

9.5.32 UPD_FULL (0x33 + 1 parameter)

This command issues a Full Frame Full Update operation to the Display Engine.

Parameter 1											
n/a	Border Update Enable	n,	n/a Display Update Waveform Mode bits 3-0								
15	14	13	12	11	10	9	8				
Display Update LUT Select bits 3-0				n/a							
7	6	5	4	3	2	1	0				

9.5.33 UPD_FULL_AREA (0x34 + 5 parameters)

This command issues an Area Defined Full Update operation to the Display Engine.

Functions performed:

1. Setup Display Engine Area Search Dimension

2. Trigger Full Area update with Parameter 1.

Parameter 2	1						
T aramotor	Pordor Undoto						
n/a	Enable	n	/a		Display Update Wav	eform Mode bits 3-0	1
15	14	13	12	11	10	9	8
	Display Update L	UT Select bits 3-0			n/	/a	
7	6	5	4	3	2	1	0
Parameter 2	2						•
		Area U	odate Pixel Rectang	ular X-Start Position	bits 11-8		
15	14	13	12	11	10	9	8
		Area U	pdate Pixel Rectang	ular X-Start Position	bits 7-0		I.
7	6	5	4	3	2	0	0
-							
Parameter 3	3					•	
		Area U	odate Pixel Rectang	ular Y-Start Position	bits 15-8		
15	14	13	12	11	10	9	8
		Area U	pdate Pixel Rectang	ular Y-Start Position	bits 7-0		
7	6	5	4	3	2	0	0
Demonstern	4				>		
Parameter 4	4						
		Ar	ea Update Pixel Rec	tangular Width bits 1	5-8		
15	14	13	12	11	10	9	8
		. Ai	rea Update Pixel Re	ctangular Width bits	7-0		
7	6	5	4	3	2	0	0
Denemator	-						
Parameter :	0						
		Are	ea Update Pixel Rec	angular Height bits 1	15-8		
15	14	13	12	11	10	9	8
		Ar	ea Update Pixel Rec	tangular Height bits	7-0		i.
7	6	5	4	3	2	0	0

9.5.34 UPD_PART (0x35 + 1 parameter)

This command issues a Partial Update operation to the Display Engine. This operation affects changed pixels only.

Functions performed: 1. Trigger Partial update with Parameter 1

Parameter 1							
n/a	Border Update Enable	n/	/a		Display Update Wav	eform Mode bits 3-0	
15	14	13	12	11	10	9	8
	Display Update L	UT Select bits 3-0		n/a			
7	6	5	4	3	2	1	0
9.5.35 UPD_PART_AREA (0x36 + 5 parameters)

This command issues an Area defined Partial Update operation to the Display Engine. This operation affects changed pixels only.

Functions performed:

- 1. Setup Display Engine Area Search Dimension
- 2. Trigger Full Area update with Parameter 1.

Parameter	1							
n/a	Border Update Enable	n	/a	Display Update Waveform Mode bits 3-0				
15	14	13	12	11	10	9	8	
	Display Update L	UT Select bits 3-0			n/	a		
7	6	5	4	3	2	1	0	
Parameter	2							
		Area U	odate Pixel Rectangu	ular X-Start Position	bits 11-8			
15	14	13	12	11	10	9	8	
	1	Area U	pdate Pixel Rectang	ular X-Start Position	bits 7-0		L	
7	6	5	4	3	2	0	0	
	_			<u>_</u>				
Parameter	3			— — — —				
		Area U	odate Pixel Rectangu	ular Y-Start Position	bits 15-8			
15	14	13	12	11	10	9	8	
		Area U	pdate Pixel Rectang	ular Y-Start Position	bits 7-0			
7	6	5	4	3	2	0	0	
Devementer	4							
Parameter	4							
		Area U	pdate Pixel Rectang	ular X-End Position I	bits 15-8			
15	14	13	12	11	10	9	8	
		Area L	Jpdate Pixel Rectang	Jular X-End Position	bits 7-0			
7	6	5	4	3	2	0	0	
Parameter	5				/			
		Area U	pdate Pixel Rectang	ular Y-End Position I	bits 15-8			
15	14	13	12	11	10	9	8	
		Area L	Jpdate Pixel Rectang	ular Y-End Position	bits 7-0			
7	6	5	4	3	2	0	0	

9.5.36 UPD_GDRV_CLR (0x37 + 0 parameters)

This command issues a display sequence output on the Gate Driver only. This command is used to clear the unknown state of the Gate Driver display at power-up.

9.5.37 UPD_SET_IMGADR (0x38 + 2 parameters)

This command sets the Display Engine Image Buffer Start Address.

Param	neter 1								
				Image Buffer Star	t Address bits 15-8				
15	5	14	13	12	11	10		9	8
				Image Buffer Sta	rt Address bits 7-0				
7	7	6	5	4	3	2		1	0
Param	neter 2								
				Image Buffer Star	Address bits 31-24				
15	5	14	13	12	11	10		9	8
	- 1	0		Image Buffer Start	t Address bits 23-16		Т		
/	/	6	5	4	3	2		1	0

Chapter 10 Registers

This section discusses how and where to access the S1D13521 registers. It also provides detailed information about the layout and usage of each register.

10.1 Register Access

The S1D13521 registers are 16-bit wide. They can be accessed using the Command Interface

10.1.1 Register Access using Command Interface

Registers may be accessed using the command interface with the following sequences.

For single 16-bit register reads:

Tx Count	16-bit Indirect Host						
0	Write Code[15:0] <= 0x0010						
1	Write Register Address[15:0]						
2	Read						

Table 10-1: Register Read Sequence

For single 16-bit register writes:

Table 10-2: Register Write Sequence

Tx Count	16-bit Indirect Host
0	Write Code[15:0] <= 0x0011
1	Write Register Address[15:0]
2	Wr <mark>ite</mark>

Note

Only single register accesses are supported (i.e. register address is not auto incremented to the next register address).

Address Range	Register Type	Description				
0000h to 000Fh	Asynchronous	System Configuration Registers				
0010h to 001Fh	Asynchronous	Clock Configuration Registers				
0020h to 002Fh	Asynchronous	Component Configuration				
0100h to 010Fh	Synchronous	Memory Controller Configuration				
0140h to 015Fh	Synchronous	Host Interface Memory Access Configuration				
0200h to 020Fh	Synchronous	SPI Flash Memory Interface				
0210h to 011Fh	Synchronous	I2C Thermal Sensor Interface Registers				
0220h to 022Fh	Synchronous	3-Wire Chip Interface Registers				
0230h to 023Fh	Synchronous	Power Pin Control Configuration Registers				
0240h to 024Fh	Synchronous	Interrupt Configuration Registers				
0250h to 025Fh	Synchronous	GPIO Control Registers				
0300h to 03FFh	Synchronous	Display Engine Reg <mark>is</mark> ters				

Table 10-3: Register Mapping

10.2 Register Set

The S1D13521 registers are listed in the following table.

Table 10-4: S1D13521 Register	Set
-------------------------------	-----

Register	Pg	Register	Pg
Syste	em Configu	ration Registers	
REG[0000h] Revision Code Register	79	REG[0002h] Product Code Register	79
REG[0004h] Config Pin Read Value Register	79	REG[0006h] Power Save Mode Register	80
REG[0008h] Software Reset Register	80	REG[000Ah] System Status Register	81
Cloc	k Configu	ation Registers	
REG[0010h] PLL Configuration Register 0	83	REG[0012h] PLL Configuration Register 1	83
REG[0014h] PLL Configuration Register 2	84	REG[0016h] Clock Configuration Register	84
REG[0018h] Pixel Clock Configuration Register	85	REG[001Ah] I2C Thermal Sensor Clock Configuration Register	86
Ca	omponent	Configuration	
REG[0020h] Peripheral Device Configuration Register	87		
Memo	ory Control	ler Configuration	
REG[0100h] SDRAM Configuration Register	88	REG[0102h] SDRAM Init Register	89
REG[0104h] SDRAM State Trigger Register	90	REG[0106h] SDRAM Refresh Clock Configuration Register	91
REG[0108h] SDRAM Read Data Tap Delay Select Registe	er 91	REG[010Ah] SDRAM Extended Mode Configuration Register	92
REG[010Ch] SDRAM Controller Software Reset Register	93		
Host Interfa	ce Memory	Access Configuration	
REG[0140h] Host Memory Access Configuration and State 94	us Register	REG[0142h] Host Memory Access Triggers Register	95
REG[0144h] Host Raw Memory Access Address Register	0 96	REG[0146h] Host Raw Memory Access Address Register 1	96
REG[0148h] Host Raw Memory Access Count Register 0	96	REG[014Ah] Host Raw Memory Access 16-bit Access Count R	egister 96
REG[014Ch] Packed Pixel Rectangular X-Start Register	97	REG[014Eh] Packed Pixel Rectangular Y-Start Register	97
REG[0150h] Packed Pixel Rectangular Width Register	97	REG[0152h] Packed Pixel Rectangular Height Register	97
REG[0154h] Host Memory Access Port Register	98	REG[0156h] Host Memory Checksum Register	98
SP	I Flash Me	mory Interface	
REG[0200h] SPI Flash Read Data Register	99	REG[0202h] SPI Flash Write Data Register	99
REG[0204h] SPI Flash Control Register	99	REG[0206h] SPI Flash Status Register	101
REG[0208h] SPI Flash Chip Select Control Register	<mark>1</mark> 02		
I2C There	mal Senso	r Interface Registers	
REG[0210h] I2C Thermal Sensor Configuration Register	103	REG[0212h] I2C Thermal Sensor Status Register	103
REG[0214h] I2C Thermal Sensor Read Trigger Register	104	REG[0216h] I2C Thermal Sensor Temperature Value Register	104
3-Wi	re Chip Inte	erface Registers	
REG[0220h] 3-Wire Chip Configuration Register	105	REG[0222h] 3-Wire Chip Access Status Register	105
REG[0224h] 3-Wire Chip Address and Write Data Byte Re	gister 106	REG[0226h] 3-Wire Chip Read Data Byte Register	106
Power Pin	Control Co	onfiguration Registers	
REG[0230h] Power Pin Control Register	107	REG[0232h] Power Pin Configuration Register	108
REG[0234h] Power Pin Timing Delay 0-1 Register	110	REG[0236h] Power Pin Timing Delay 1-2 Register	110
REG[0238h] Power Pin Timing Delay 2-3 Register	110		
Interr	upt Config	uration Registers	
REG[0240h] Interrupt Raw Status Register	111	REG[0242h] Interrupt Masked Status Register	113
REG[0244h] Interrupt Control Register	115		
0	SPIO Contr	ol Registers	
REG[0250h] GPIO Configuration Register	117	REG[0252h] GPIO Status/Control Register	117
REG[0254h] GPIO Interrupt Enable Register	118	REG[0256h] GPIO Interrupt Status Register	118
Comma	Ind RAM C	ontroller Registers	
REG[0290h] Command RAM Controller Configuration Reg	jister 119	REG[0292h] Command RAM Controller Address Register	119

Register	Pg	Register	Pg						
REG[0294h] Command RAM Controller Access Port Register	119								
Command Sec	quence	r Controller Registers							
REG[02A0h] Command Sequencer Controller Index Register	120	REG[02A2h] Command Sequencer Controller Data Port Regist	er 120						
Display Engine: Display Timing Configuration									
REG[0300h] Frame Data Length Register	121	REG[0302h] Frame Sync Length Register	121						
REG[0304h] Frame Begin/End Length Register	121	REG[0306h] Line Data Length Register	122						
REG[0308h] Line Sync Length Register	122	REG[030Ah] Line Begin/End Length Register	122						
Display Eng	ine: Dr	iver Configurations							
REG[030Ch] Source Driver Configuration Register	123	REG[030Eh] Gate Driver Configuration Register	<mark>12</mark> 5						
Display Engine: Memo	ory Re	gion Configuration Registers							
REG[0310h] Image Buffer Start Address Register 0	126	REG[0312h] Image Buffer Start Address Register 1	126						
REG[0314h] Update Buffer Start Address Register 0	126	REG[0316h] Update Buffer Start Address Register 1	126						
Display Eng	gine: C	omponent Control							
REG[0320h] Temperature Device Select Register	127	REG[0322h] Temperature Value Register	127						
REG[0324h] DWELL Time Configuration Register	127	REG[0326h] Border Configuration Register 0	128						
REG[0328h] Border Configuration Register 1	128	REG[032Ah] Power Control Configuration Register	129						
REG[032Ch] General Configuration Register	130	REG[032Eh] LUT Mask Register	131						
Display Engin	e: Con	trol/Trigger Registers							
REG[0330h] Update Buffer Configuration Register	132	REG[0332h] <mark>Update Bu</mark> ffer Pixel Set Value Register	133						
REG[0334h] Display Engine Control/Trigger Register	133								
Display Engine:	Update	Buffer Status Registers							
REG[0336h] Lookup Table Status Register	135	REG[0 <mark>338</mark> h] Display Engine Busy Status Register	135						
Display En	gine: lı	nterrupt Registers							
REG[033Ah] Display Engine Interrupt Raw Status Register	138	REG[033Ch] Display Engine Interrupt Masked Status Register	141						
REG[033Eh] Display Engine Interrupt Enable Register	144								
Display Engine: Par	tial Upo	late Configuration Register							
REG[0340h] Area Update Pixel Rectangular X-Start Register	147	REG[0342h] Area Update Pixel Rectangular Y-Start Register	147						
REG[0344h] Area Update Pixel Rectangular X-End / Horizonta	l Size	REG[0346h] Area Update Pixel Rectangular Y-End / Vertical Si	ze						
Register	147	Register	147						
REG[0348h] Host Pixel Rectangular X-Start Register	148	REG[034Ah] Host Pixel Rectangular Y-Start Register	148						
REG[034Ch] Host Pixel Rectangular X-End Register	148	REG[034Eh] Host Pixel Rectangular Y-End Register	148						
Display Engine: S	erial F	ash Waveform Registers							
REG[0350h] Waveform Header Serial Flash Address Register	0 149	REG[0352h] Waveform Header Serial Flash Address Register (0 149						
REG[0354h] through REG[035Eh] are Reserved									

Table 10-4: S1D13521 Register Set (Continued)

R'S

10.3 Register Descriptions

10.3.1 System Configuration Registers

REG[0000 Default = (h] Rev 0000h	vision Co	de Register					Read Only
				Revision (Code bits 15-8			,
15		14	13	12	11	10	9	8
				These bits alway	s return 0000_0000b			
7		6	5	4	3	2	1	0
bits 7-0		Th	ese bits alway	s return 0000_	0000b.			
oits 15-8		Re	vision Code b	oits [7:0] (Read	Only)			
		Th	ese bits indica	ate the revision	code.			
		Th	e revision cod	le for the S1D1	3521 is 00h.			
REG[0002	h] Pro	duct Coo	de Register		•			
Default = 0)047h							Read Only
				Product C	Code bits 15-8			
15		14	13	12	11	10	9	8
-	i		I -	Product	Code bits 7-0		. 1	2
/		6	5	4		2	1	0
bits 15-0		Pr	oduct Code bi	ts [15:0] (Read	Only)			
		Th	ese bits indica	ate the product	code.			
		Th	e product cod	le for the S1D1	35 <mark>21 is 0047h.</mark>			
			•					
REG[0004	h] Cor	nfig Pin F	Read Value R	egister				
Default = 0)00Xh							Read Only
					n/a			
15		14	13	12	11	10	9	8
_	I.	_	n/a	1 .		- 1	CNF[2:0] Status	_
7		6	5	4	3	2	1	0
bits 2-0		Cl	VF[2:0] Status	(Read Only)				
		Th	lese bits return	the status of the	he configuration	pins CNF[2:0]. For a function	onal descrip-
		tio	n of each CN	F[2:0] pin, see	Section 4.2.10, "	Miscellaneou	s" on page 20.	
					,		1 0	

REG[0006h] Default = 000	REG[0006h] Power Save Mode RegisterDefault = 0001hRead/Write							
			n	ı/a				
15	14	13	12	11	10	9	8	
			n/a				Power Save Mode Enable	
7	6	5	4	3	2	1	0	

bit 0

Power Save Mode Enable

This bit controls power save mode.

When this bit = 0b, power save mode is disabled.

When this bit = 1b, power save mode is enabled and all clocks are gated off. (default)

This bit in combination with the PLL Power Down (REG[0016h] bit 1) and PLL Bypass (REG[0016h] bit 0) bits, define the different power states of the S1D13521. The following table summarizes the possible states of the S1D13521.

Table 10-5: S1D13521 Power States Summary

Power State	Power Save Mode Enable (REG[0006h] bit 0)	PLL Power Down (REG <mark>[0016h]</mark> b <mark>it</mark> 1)	PLL Bypass (REG[0016h] bit 0)
OFF	1b	1b	1b
SLEEP	1b	1b	1b
STANDBY (PLL) (See Note)	1b	Ob	0b
RUN (PLL)	0b	0b	0b
RUN (CLKI)	Ob	1b	1b

Note

When STANDBY (PLL) is selected, all internal clocks are gated off but the PLL remains running. This is done to avoid waiting for the PLL to become stable (PLL lock time) before returning to the RUN (PLL) state. There is no STANDBY (CLKI) state.

REG[0008h] Software Reset Register Default = 0000h Write Only								
n/a								
15	14	13	12	11	10	9	8	
n/a								
7	6	5	4	3	2	1	0	

bit 0

Software Reset (Write Only)

This bit performs a software reset of the S1D13521 which sets all registers to their default states and all pins to their RESET# states.

Writing a 0b to this bit has no hardware effect.

Writing a 1b to this bit initiates a software reset of the S1D13521.

REG[000Ah]	System Statu	is Register					
Default = 000	0h						Read/Write
3-Wire Busy Status <mark>(RO)</mark>	Power Management Busy Status (RO)	n/a	Power Save Status bits 2-0			SDRAM Self Refresh Mode Status (RO)	Power Management Power Sequence Status (RO)
15	14	13	12	11	10	9	8
I2C Busy Status (RO)	SPI Busy Status (RO)	Host Interface Busy Status (RO)	SDRAM Controller Busy Status (RO)	Host Memory Access Busy Status (RO)	Display Engine Busy Status (RO)	SDRAM Initialized (RO)	PLL Lock (RO)
7	6	5	4	3	2	1	0
bit 15	3-W This Wh Wh	Vire Busy Statu s bit indicates t en this bit = 0t en this bit = 1t	s (Read Only) the status for 3 o, 3-Wire is no o, 3-Wire is but	-Wire. t busy. sy.		X	
bit 14	Pow This Wh Wh	ver Manageme s bit indicates t en this bit = 0t en this bit = 1t	nt Busy Status the status of th o, the Power M o, the Power M	(Read Only) e Power Mana anagement log	igement lo <mark>gic.</mark> gic is not busy. gic i <mark>s</mark> busy.	<u>い</u>	
bits 12-10	Pow	ver Save Status	s bits [2:0]				
	The	se bits indicate	the power say	ve status of the	\$1D13521.		
	Table 10-6 : Power Save Status						
		REG[000A	h] bits 12-10	Power Sa	ve Status		
		0	00b	Unkn	nown		
		0	01b	Normal C	Operation		
		0	10b	Standby	y Mode		
		0	11b	Sleep	Mode		
		100b	~ 111b	Rese	erved		
					/		
bit 9 SDRAM Self Refresh Mode Status (Read Only) This bit indicates whether the SDRAM controller is in self refresh mode. SDRAM self refresh mode is controlled using the SDRAM Enter Self Refresh Trigger bit (REG[0104h] bit 0) and the SDRAM Exit Self Refresh Trigger bit (REG[0104h] bit 1). When this bit = 0b, the SDRAM controller is not in self refresh mode. When this bit = 1b, the SDRAM controller is in self refresh mode.							
bit 8	 Power Management Power Sequence Status (Read Only) This bit provides the status of the power management sequence. For further information, see Section 6.6, "Power Pin Interface" on page 43. When this bit = 0b, it is currently in a power off state. (default) When this bit = 1b, it is currently in a power on state. 						information,
bit 7	t 7 I2C Busy Status (Read Only) This bit indicates whether the I2C interface is busy. When this bit = 0b, the I2C interface is idle (not busy). When this bit = 1b, the I2C interface is busy.						

bit 6	SPI Busy Status (Read Only)This bit indicates whether the SPI interface is busy.When this bit = 0b, the SPI interface is idle (not busy).When this bit = 1b, the SPI interface is busy.
bit 5	Host Command Interface Busy Status (Read Only) This bit indicates whether the Host Command interface is busy. When this bit = 0b, the Host Command interface is idle (not busy). When this bit = 1b, the Host Command interface is busy.
bit 4	SDRAM Controller Busy Status (Read Only) This bit indicates whether the SDRAM controller is busy. When this bit = 0b, the SDRAM controller is idle (not busy). When this bit = 1b, the SDRAM controller is busy.
bit 3	Host Memory Access Busy Status (Read Only) This bit indicates whether a Host Memory Access is taking place. When this bit = 0b, a Host Memory Access is not taking place (not busy). When this bit = 1b, a Host Memory Access is taking place (busy).
bit 2	Display Engine Busy Status (Read Only) This bit indicates whether the Display Engine is busy. When this bit = 0b, the Display Engine is idle (not busy). When this bit = 1b, the Display Engine is busy.
bit 1	SDRAM Initialized (Read Only) This bit indicates whether the SDRAM has been initialized. The SDRAM initialization sequence is triggered by the SDRAM Initialization Trigger bit, REG[0102h] bit 0. When this bit = 0b, the SDRAM has not been initialized. When this bit = 1b, the SDRAM has been initialized.
bit 0	PLL Lock (Read Only) This bit indicates whether the PLL output is stable (locked). The S1D13521 synchronous registers (see Table 10-3: "Register Mapping," on page 76) and the external SDRAM must not be accessed before the PLL output is stable. When this bit = 0b, the PLL output is not stable. When this bit = 1b, the PLL output is stable.

10.3.2 Clock Configuration Registers

REG[0010	h] PLL	Configu	uration Regi	ster 0								Pa	ad/M/rita
	00001				DI L O - t		it. 7.0						au/ white
15	I	14	12	1	PLL Set	ing u b I	Its 7-0	I	10	1	0	1	0
10	n/a	14	13		12		 M-D	ivider bits	5-0		9		0
7	l l	6	5		4		3		2		1	1	0
bits 15-8	ts 15-8 PLL Setting 0 bits [7:0] These bits must be set to F8h.												
bits 5-0		M Th Th 20	-Divider bits hese bits dete hese bits mus MHz and 66	[5:0] rmine t be set 5.5MHz Table 1	the divide t such tha z. 20-7: PLL	t the) betwee internal Divide Se	en CLK input o	I and th clock to	e actua the PL	al input L (PLI	clock to .CLK) i	o the PLL. s between
			REG	[10h] b	its 5-0		M-Div	vider R	atio				
				0h				1:1					
				0311				4 .					
				•				•					
				•									
				20h	(33:1					
				21h to 3	Fh		Re	eserved	1 V				
REG[0012	h] PLL	Configu	uration Regi	ster 1				<u>}</u>					
Default = 0	1000n				DI LO - M							RE	ad/write
15	1	14	13		12	ng i bi	11 15-8	Ì	10	I	9	ĺ	8
	I				PLL Set	ting 1 b	its 7-0					I	0
7		6	5		4		3		2		1		0
bits 15-0		PL Tř	L Setting 1 lese bits mus	bits [15 It be se	5:0] t to 2880ł	1.							

Default = 00	00h						Read/Write
n/a				L-Counter bit	s 6-0		
15	14		13	12 11	10	9	8
				PLL Setting 2 bits 7-0			
7	6		5	4 3	2	1	0
ts 14-8		L-Counte These bits following PLL Outp	r bits [6:0] s are used to co s formula. put = (L- = LL	onfigure the PLL O Counter + 1) x PLI x PLLCLK	utput (in MHz) : LCLK	and must be set	according to the
		Where:					
		PLL	Output is the d	esired PLL output	frequency (in N	1Hz).	
		L-Co	unter is the va	lue of this register ((in decimal).		
		PLLC	CLK is the inte	rnal input clock to	the PLL (in MI	Iz).	
Target Fi (M	requency Hz)	LL	CLKI Input Clock (MHz)	M-Divider REG[0010h] bits 5-	M-Divide Ratio	PLLCLK (MHz)	POUT (MHz)
1:	33	4	33	00h	1:1	33	132
its 7-0 REG[0016h] Default = 00] Clock Co <mark>02</mark> h	PLL Setti These bit	ng 2 bits [7:0] s must be set t on Register	o 00h.	ð,	•	Read/Write
				n/a			System Clock
	1	1			1		Divide Select
15	14		13	12 11	10	9 PLL Power Dov	8 ND PLL Bypass Mor
			n/a			Enable	Enable
7	6		5	4 3	2	1	0
it 8		System C This bit s either the	lock Divide Selects the divide PLL output of fol bit 0. The	elect le ratio used to gen r the CLKI input de maximum frequen	erate the system epending on the	n clock which i PLL Bypass S n clock is 66 5	s derived from elect bit, Mbz For furth

bit 1	PLL Power Down Enable This bit controls the PLL. Once the PLL is placed in a powered down state, enabling it will require a minimum of 1 ms before the PLL output is stable. The status of the PLL can be checked using the PLL Lock bit, REG[000Ah] bit 0. For further details on the clock structure, see Section Chapter 7, "Clocks" on page 45. When this bit = 0b, the PLL is in active mode and PLL output is stable once REG[000Ah] bit 0 = 1b. When this bit = 1b, the PLL is in power down mode. (default)
bit 0	PLL Bypass Mode Enable This bit controls PLL Bypass Mode which determines whether the PLL output or the CLKI input is used as the internal clock. For further details on the clock structure, see Sec- tion Chapter 7, "Clocks" on page 45. When this bit = 0b, PLL Bypass Mode is disabled (PLL output is used). When this bit = 1b, PLL Bypass Mode is enabled (CLKI is used).

REG[0018h] Default = 000	Pixel Clock C Oh	onfiguration	X		Read/Write			
			n,	/a				
15	14	13	12	11	10	9	8	
n/a Pixel Clock Divide Disable					Pixel Clock Divid	le Select bits 3-0		
7	7 6 5 4 3 2 1					0		

bit 4

Pixel Clock Divide Disable

This bit controls whether the pixel clock source is divided or not. When this bit = 0b, the Pixel Clock Divide Select bits (REG[0018h] bit 3-0) are used to determine the pixel clock. When this bit = 1b, the pixel clock source is pot divided (1:1). Note that this setting is po

When this bit = 1b, the pixel clock source is not divided (1:1). Note that this setting is not recommended for normal operations.

bits 3-0 Pixel Clock Divide Select bits [3:0] These bits select the divide ratio for the Pixel Clock which is derived from either the PLL output or CLKI depending on the PLL Bypass Mode Enable bit, REG[0016h] bit 0. For further details on the clock structure, see Section Chapter 7, "Clocks" on page 45.

REG[0018h] bits 3-0	Pixel Clock Divide Ratio	REG[0018h] bits 3-0	Pixel Clock Divide Ratio
0000b	1:1.5	1000b	1:9
0001b	1:2	1001b	1:10
0010b	1:3	1010b	1:11
0011b	1:4	1011b	1:12
0100b	1:5	1100b	1:13
0101b	1:6	1101b	1:14
0110b	1:7	1110b	1:16
0111b	1:8	1111b	1:64

REG[001Ah] I2C Thermal Sensor Clock Configuration Register Default = 0007h Read/Write							
	n/a						
15	14	13	12	11	10	9	8
n/a I2C Thermal Sensor Clock Divide Select bits 3-0							
7	6	5	4	3	2	1	0

bits 3-0

I2C Thermal Sensor Clock Divide Select bits [3:0]

These bits select the divide ratio for the I2C Thermal Sensor Clock which is derived from either the PLL output or CLKI depending on the PLL Bypass Mode Enable bit, REG[0016h] bit 0. For further details on the clock structure, see Section Chapter 7, "Clocks" on page 45.

The divide ratio is calculated using the following formula. I2C Thermal Sensor Clock Divide Ratio = 1 : (REG[001Ah] bits 3-0+1)

Note

This clock must be set such that it satisfies the following equation: Clock Divide = System Clock $(50Mhz) / (16 \times 400Khz)$

10.3.3 Component Configuration

REG[0020h] Default = 00] Peripheral I 00h	Device Con	figurat	ion Registe	er			Read/Write
				r	n/a			
15	14	13		12	11	10	9	8
				n/a	·			Power Line Management Select
7	6	5	1	4	3	2	1	0
hit ()	P	wer Line M	lanager	nent Select			•	

b1t 0

Power Line Management Select

This bit selects whether internally generated timing is used for power pin management or whether a Dialog DA8590 IC or compatible device is used power management. This bit must be set to 0b when a Dialog DA8590 IC or compatible device is not present. When this bit = 0b, internal timing is used for power pin management. When this bit = 1b, a Dialog DA8590 IC or compatible device is used for power management.

10.3.4 Memory Controller Configuration

REG[0100h]	SDRAM Conf	iguration Reg	ister					
Default = 507	0h						Read/Write	
SDRAM Power Down Disable	SDRAM	Refresh Cycle Time	e bits 1-0	SDRAM Refres	h Rate bits 1-0	SDRAM Row Ac	SDRAM Row Active Time bits 1-0	
15	14	13	13 12		10	9	8	
16-bit SDRAM Enable	SDRAM tRP Latency Select	SDRAM tRCD Latency Select	SDRAM tRCD SDRAM tCL Latency Select Latency Select		SDRAM Colum	n Address Count s 1-0	SDRAM Burst Type Select	
7	6	5	4	3	2	1	0	
bit 15	SDI This SDI Wh Wh	RAM Power D s bit controls th RAM clock wh en this bit = 0h en this bit = 1h	own Disable he SDRAM po hen the SDRAI b, the SDRAM b, the SDRAM	wer down fun M is idle. power down f power down f	ction which d unction is ena unction is disa	ynamically disa bled. able <mark>d</mark> .	ables the	
bits 14-12	SDI The	RAM Refresh se bits specify Refresh cycle	Cycle Time bit the SDRAM I time = REG[0	ts [2:0] Refresh Cycle 100h] bits 14-	Time (t R FC) 12 + 4	using the follow	wing formula.	
bits 11-10	SDI The	RAM Refresh se bits specify	Rate bits [1:0] the SDRAM r	efresh rate for	8192 rows.			
		Table 10	-10: SDRAM	l Refresh Rate	Selection			
		REG[0100	h] bits 11-10	Refresi	Rate			
		C)0b	64 r	ns			
		0)1b	128	ms			
		1	l0b	256	ms			
		1	1b	512	ms			
bits 9-8	SDI The ope	RAM Row Act se bits specify ned row to be Table 10-11 :	tive Time bits the Row Activities issued a precha SDRAM Row	[1:0] ve Time (tRAS arge. Active Time (t) which defin RAS) Selectio	es the minimur n	n time for an	
		KEGLOIO		F clo				
				5 clocks				
				7 CIO	cks			
		1	1b	8 Clo	CKS			
bit 7	16-l This Wh Wh	bit SDRAM End S bit specifies where S bit specifies where S bit	nable whether 16 or 3 o, 32-bit SDRA o, 16-bit SDRA	32-bit SDRAM AM mode is sel AM mode is sel	I is selected. ected. ected.			

bit 6	SDRAM tRP Latency This bit selects the Ro can be activated again When this bit = 0b, th When this bit = 1b, th	v Select w Precharge Time which is the h. e row precharge time is 2 cloc e row precharge time is 3 cloc	e precharge time required before a row ks. ks.
bit 5	SDRAM tRCD Laten This bit selects the Ro When this bit = 0b, th When this bit = 1b, th	cy Select ow to Column Latency. e row to column latency is 2 c e row to column latency is 3 c	locks. locks.
bit 4	SDRAM tCL Latency This bit selects the Co When this bit = 0b, th When this bit = 1b, th	v Select blumn Read to Data Available e column read to data availabl e column read to data availabl	Latency. e latency is 2 clocks. e latency is 3 clocks.
bits 2-1	SDRAM Column Add This bit specifies the r Table 10-12 : SL	dress Count bits [1:0] number of column addresses u DRAM Column Address Count	sed for the SDRAM. Selection
	REG[0100h]	bits 2-1 Column Address	Count
	00b	256	
	01b	512	►
	10b	1024	
	11b	2048	

bit 0

SDRAM Burst Type Select

This bit selects the type of burst used for SDRAM accesses. When this bit = 0b, full page burst is selected. This setting is used for standard SDRAM. When this bit = 1b, fixed 8-burst is selected. This setting is used for mobile SDRAM.

REG[0102h Default = 00] SDRAM Ini t 000h	t Register						Read/Write
				n/a				SDRAM Initialization Complete (RO)
15	14	13		12	11	10	9	8
			n/a				SDRAM Initialization Wait Select	SDRAM Initialization Trigger (WO)
7	6	5		4	3	2	1	0
bit 8	S	DRAM Initia	lizatio	on Complete	(Read Only)			

This bit indicates the initialization status of the SDRAM. Once SDRAM has been initialized, this bit will remain high until the S1D13521 is reset.

When this bit = 0b, the SDRAM has not been initialized.

When this bit = 1b, the SDRAM has been initialized.

bit 1	SDRAM Initialization Wait Select
	This bit selects the minimum amount of wait time required by the SDRAM before starting
	the initialization sequence.
	When this bit = 0b, the minimum wait time is 100μ s (i.e. Micron SDRAM).
	When this bit = 1b, the minimum wait time is $200\mu s$ (i.e. Samsung SDRAM).
bit 0	SDRAM Initialization Trigger (Write Only)
	This bit triggers the SDRAM initialization sequence. The initialization status of the
	SDRAM is indicated by the SDRAM Initialization Complete bit, REG[0102h] bit 8.
	Writing a 0b to this bit has no effect.
	Writing a 1b to this bit initiates the SDRAM initialization sequence.

REG[0104h]	SDRAM State	e Trigger Regis	ster				
Default = 000	00h						Read/Write
			n/a				SDRAM Self Refresh Mode State (RO)
15	14	13	12	11	10	9	8
		n/	а			SDRAM Exit Self Refresh Trigger (WO)	SDRAM Enter Self Refresh Trigger (WO)
7	6	5	4	3	2	0	0
bit 8 bit 1	SDI This Wh Wh SDI This Wri	RAM Self Refr s bit indicates w en this bit = 0b en this bit = 1b RAM Exit Self s bit triggers th ting a 0b to thi ting a 1b to thi	esh Mode Stat whether the SE , the SDRAM , the SDRAM Refresh Trigg e sequence tha s bit has no eff s bit triggers th	e (Read Only) DRAM is in Se is not in self r is in self refre er (Write Only it removes (ex ect. ie exit self refu	elf Refresh mode efresh mode (1 sh mode. 7) its) the SDRA resh sequence.	de or not. normal operati M from Self R	ng mode). efresh mode.
bit 0	SDI This Wri Wri	RAM Enter Sel s bit triggers th ting a 0b to thi ting a 1b to thi	f Refresh Trig e sequence to s bit has no eff s bit triggers th	ger (Write On places (enters) fect. he enter self re	ly) the SDRAM fresh sequence	to Self Refresł e.	n mode.

 $\langle \rangle$

REG Defa	[010 ult =	6 h] SDF 0177h	RAM R	efre	sh Clock Co	nfiguration Re	egister				Re	ad/Write
					SI	DRAM Refresh Clock	Divide Select bits 1	5-8				
	15		14		13	12	11	10		9		8
					S	DRAM Refresh Clock	k Divide Select bits 7	-0	I			
	7		6		5	4	3	2		0		0
bits 1	5-0			SDR	AM Refresh	Clock Divide S	Select bits [15:	0]				
				Thes	se bits select t	he divide used	to determine t	he SDRA	M Refre	esh Cloc	k fr <mark>equ</mark>	ency.
			,	Thes	se bits should	be set such that	t the resulting	refresh clo	ock is ap	proxi <mark>m</mark>	ately 64	4 <mark>KHz.</mark> For
				furth	er informatio	n on the clock	structure, see	Section C	hapter 7	, "Clock	<mark>(s"</mark> on p	ag <mark>e</mark> 45.
]	Refresh Clock	c Divide = REC	G[0106h] bits	15-0+1				
			,	The	nofnoch alaak	in coloulated u	aing the fellow	in a farma				
				The	Refresh clock	$r_{\rm frequency} = C$	'I KI frequency	ng ionn • ÷ Refres	ula.	Divide		
				1	Reffesti clock	frequency – C		y + Refies				
				For e	example, the o	default register	value of 0177	h results in	n the fol	lowing:	refresh	frequency
				whe	n CLKI is 241	MHz.				0		1 5
]	Refresh clock	frequency	$= 24 MHz \div$	375				
							= 64KHz /					
REG Defa	[0108	Shj SDF 0000b	KAM K	ead	Data Tap De	lay Select Reg	gister				Re	ad/\//rita
Doiu	un –	000011				n	/2					
	15	1	14	1	13	12	11	10	1	9	1	8
					SDRAM Read	SDRAM Read						-
		n/a			Data Sampling	Data Sampling Clock Invert	Reserved			Reserved		
					Select	Enable						
	7		6		5	4	3	2		1		0
bit 5				SDR	AM Read Da	ta Sampling S	elect					
				This	bit selects wl	hen SDRAM re	ead data is sam	pled.				
				Whe	on this bit $= 0$	o, SDRAM rea	d data is samp	led on the	positive	e edge.		
				<mark>Wh</mark> e	n this b <mark>it</mark> = 11	o, SDRA <mark>M r</mark> ea	d da <mark>t</mark> a is samp	led on the	negativ	e edge.		
bit 4				S <mark>DR</mark>	AM Read Da	ta Sampling C	lock Invert En	able				
				This	bit controls v	whether the san	npling clock us	sed for SE	DRAM d	lata read	ls is inv	erted.
				Whe	n this bit $= 0$	b, the sampling	clock is not in	overted.				
				Whe	n this bit $= 11$	b, the sampling	clock is inver	ted.				
hit 3				Rese	erved							
510 5				This	bit must be s	et to 0b.						
hite?	-0		· .	Rese	erved							
0105 2				Theo	se hits must h	e set to 000b						
				1 1100								

REG[010Ah] Default = 000	SDRAM Exte)0h	nded Mode C	onfiguration I	Register			Read/Write
n/a	SDRAM Driver	Strength bits 1-0	Temperature Co Refresh	ompensated Self bits 1-0	Partial	Array Self Refresh I	oits 2-0
15	14	13	12	11	10	9	8
		n/a			SDRAM S	ize bits 1-0	Extended Mode Register Program on Initialization Enable
7	6	5	4	3	2	1	0
/	0	Э	4	3	2		

bits 14-13

SDRAM Driver Strength bits [1:0]

• These bits only have an effect when the Extended Mode Register Program On Initialization Enable bit is set to 1b, REG[010Ah] bit 0 = 1b. These bits set the value for Driver Strength (DS) that is programmed into the extended mode register of the mobile SDRAM.

Table 10-13 :	SDRAM Driver	Strength Selection
10000 10 10 1		Strength Sereener

REG[010Ah] bits 14-13	Driver Strength
00b	Full Strength
01b	Half Strength
10b	Quart <mark>e</mark> r Strength
11b	Eighth Strength

bits 12-11	Temperature Compensated Self	Refresh bits [1:0]	
	These bits only have an effect w	hen the Extended Mode Reg	gister Program On Initializa-
	tion Enable bit is set to 1b, REG	[010Ah] bit $0 = 1b$. Mobile	SDRAM allows the self
	refresh rate to be varied based or	n the temperature of the SDI	RAM. These bits set the value
	for Temperature Compensated S	elf Refresh (TCSR) that is p	programmed into the extended
	mode register of the mobile SDI	R <mark>A</mark> M.	-
bits 10-8	Partial Array Self Refresh bits [2:0]	
	These bits only have an effect w	hen the Extended Mode Reg	gister Program On Initializa-
	tion Enable bit is set to 1b, REG	;[010Ah] bit 0 = 1b. These b	bits set the value for Partial
	Array Self Refresh (PASR) that	is programmed into the exte	ended mode register of the
	mo <mark>b</mark> ile SDRAM.		
bits 2-1	SDRAM Size bits [1:0]		
	These bits specify the SDRAM	size, in M bytes. This setting	g is used for bank address
	placement.		
		RAM Size Selection	
	REG[010Ah] bits 2-1	SDRAM Size	
	0.01		

REG[010Ah] bits 2-1	SDRAM Size
00b	8M bytes
01b	16M bytes
10b	32M bytes
11b	64M bytes

Extended Mode Register Program On Initialization Enable
When mobile SDRAM is used, this bit controls whether the extended mode register is programmed when the SDRAM is initialized, REG[0102h] bit 0 = 1b.
When this bit = 0b, the extended mode register is not programmed when the SDRAM is initialized.
When this bit = 1b, the extended mode register is programmed when the SDRAM is initialized.

efault = 0000h Write On 15 14 13 12 11 10 9 8 N/a SDRAM Controller 7 6 5 4 3 2 1 0 SDRAM Controller Software Reset (Write Only) This bit performs a software reset of the SDRAM controller. Writing a 0b to this bit has no effect. Writing a 1b to this bit performs a software reset of the SDRAM controller.	EG[010Ch	n] SDRAM Cor	ntroller Softwa	re Reset Regis	ter			
15 14 13 12 11 10 9 8 n/a n/a SDRAM 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 10 SDRAM Controller Software Reset (Write Only) This bit performs a software reset of the SDRAM controller. Writing a 0b to this bit has no effect. Writing a 1b to this bit performs a software reset of the SDRAM controller. Writing a 1b to this bit performs a software reset of the SDRAM controller.	efault = 00)00h						Vrite Only
7 6 5 4 3 2 1 0 10 SDRAM Controller Software Reset (Write Only) This bit performs a software reset of the SDRAM controller. Writing a 0b to this bit has no effect. Writing a 1b to this bit performs a software reset of the SDRAM controller.	15	14	13	n/a 12	11	10	9	8
7 6 5 4 3 2 1 0 t 0 SDRAM Controller Software Reset (Write Only) This bit performs a software reset of the SDRAM controller. Writing a 0b to this bit has no effect. Writing a 1b to this bit performs a software reset of the SDRAM controller. Writing a 1b to this bit performs a software reset of the SDRAM controller.				n/a				SDRAM Controller Software Rese
 SDRAM Controller Software Reset (Write Only) This bit performs a software reset of the SDRAM controller. Writing a 0b to this bit has no effect. Writing a 1b to this bit performs a software reset of the SDRAM controller. 	7	6	5	4	3	2	1	0
		Wi Wi	riting a 0b to thi	s bit has no effe s bit performs a	ect. software re	set of the SDR.	AM controller	г.

bit 0

10.3.5 Host Interface Memory Access Configuration

REG[0140h] Default = 000	Host Memory 0h	Access Conf	iguration and	I Status Regis	ster		Read/Write
Host Memory Interface Reset (WO)	n/a	Host Memory Interface Ready Status (RO)	Host Memory Interface Busy Status (RO)	n	/a	Write Rotatior	n Select bits 1-0
15	14	13	12	11	10	9	8
Packed Pixel Destination Start Address Select	n/a	Host Packed Pix	el Select bits 1-0	Host Rotate 0 and 180 Line Buffer Bypass Enable	Memory Read/Write Select	Memory A	ccess Type
7	6	5	4	3	2	1	0
bit 15	Hos This Wri Wri	t Memory Intest bit performs ting a 0b to thi ting a 1b to thi	erface Reset (V a software rese s bit has no ef s bit initiates a	Vrite Only) et of the host n fect. a software rese	nemory interfact	ce. emory interfa	ce.
bit 13	Hos This beer Wh buff Wh	t Memory Inters bit indicates to triggered (see en this bit = 0th Yer). en this bit = 1th	erface Ready S the ready statu e REG[0142h] o, the host mer o, the host mer	tatus (Read On s of the host m bit 0). nory interface nory interface	nly) nemory interfac is not ready (b) is ready for a d	e once a data usy filling or o lata transfer.	transfer has clearing the
bit 12	Hos This Whe Whe	t Memory Inte s bit indicates t en this bit $= 0t$ en this bit $= 1t$	erface Busy Status the busy status o, the host mer o, the host mer	atus (Read Onl s of the host mo nory interface nory interface	y) emory interface is idle. is busy.	2.	
bits 9-8	Wri The = 00 writ	te Rotation Set se bits only ha Db. These bits es. Table	lect b <mark>it</mark> s [1:0] ve an effect wl select the cour 510-15 : Writ	hen Packed Pix hter-clockwise te Rotation Sel	tel Access is se rotation applie ection	lected, REG[(d to host men	0140h] bits 1-0 nory interface
		REG[014	0h] bits 9 <mark>-8</mark>	Write R	otation		
		C	00b	0'	0		
		C)1b	90)°		
		1	0b	18	0°		
		1	1b	27	0°		
bit 7	Pac. Wh dest Wh buff Wh add	ked Pixel Dest en packed pixe ination start ac en this bit = 0t fer start addres en this bit = 1b ress, REG[014	ination Start A el mode is sele ldress for the r o, the destinations, REG[0310h o, the destination (4h] ~ REG[01	Address Select cted (REG[014 memory write. on start addres] ~ REG[0312 on start address 46h].	40h] bits 1-0 = s is defined by h]. s is defined by t	00b), this bit the Display E he Host raw r	determines the Engine image nemory access

bits 5-4Host Packed Pixel Select bits [1:0]These bits only have an effect when Packed Pixel Access is selected, REG[0140h] bits 1-0= 00b. These bits select the packed pixel mode used for host memory interface accesses.

REG[0140h] bits 5-4	Packed Pixel Mode
00b	2 bpp
01b	3 bpp
10b	4 bpp
11b	8 bpp

Table 10-10 : Packea Pixel Moae Selection	<i>Table 10-16 :</i>	Packed Pixel Mode Selection
---	----------------------	-----------------------------

bit 3	Host Rotate 0 and 180 Line Buffer Bypass Enable
	When the Write Rotation Select bits are set for 0° or 180° (REG[0140h] bits 9-8 = 00b or
	10b), this bit determines whether the line buffer is used or bypassed. When write rotation
	is set for 90° or 270°, the line buffer is always used.
	When this bit = 0b, the line buffer is used. $($
	When this bit = 1b, the line buffer is bypassed (not used).
bit 2	Memory Read/Write Select
	This of selects the memory read write direction.
	When this bit = 0b, the host memory interface is configured to write to memory.
	When this bit = 1b, the host memory interface is configured to read from memory.

bits 1-0 Memory Access Type Select bits [1:0] These bits select the type of memory access performed through the host memory interface.

Table 10-17 <mark>:</mark>	Memo	ry <mark>Acces</mark> s	s Typ <mark>e</mark>	Se <mark>lec</mark> tion

REG[0140h] bits 1-0	Memory Access Type
00b	Packed Pixel Access (Write Only)
01b	Raw Memory Access (Read/Write)
10 <mark>b ~ 11</mark> b	Reserved

Default = 00	00h		r	n/a			Write Only
15	14	13	12	11	10	9	8
			n/a			Host Transfer Stop Trigger	Host Transfer Start Trigger
7	6	5	4	3	2	0	0
	This Wri Wri	s bit stops the ting a 0b to th ting a 1b to th	data transfer ta iis bit has no ef iis bit triggers t	king place on fect. he current hos	the host memory inte	ory interface. rface transfer to	o stop.
oit 0	Hos This Wri Wri	t Transfer Sta s bit starts a n ting a 0b to th ting a 1b to th	rt Trigger (Wri ew data transfe iis bit has no ef iis bit triggers a	te Only) or on the host r fect. a new data trar	nemory interfa	ace. 1 the host memo	ory interface.

REG[0144h Default = 00] Host Raw N 00h	lemory Acce	ess Address Reg	ister 0			Read/Write
			Host Raw Memory Acc	cess Address bits 15-8			
15	14	13	12	11	10	9	8
			Host Raw Memory Ac	cess Address bits 7-0			
7	6	5	4	3	2	0	0
2EC[01/6h	1 Host Raw M	lemory Acce	se Address Rea	istor 1			
Default = 00	00h	lemory Acce	ss Address Neg				Read/Write
			Host Raw Memory Acc	ess Address bits 31-24	4		
15	14	13	12	11	10	9	8
			Host Raw Memory Acc	ess Address bits 23-10	6		
7	6	5	4	3	2	0	0
EG[0146h] EG[0144h]	bits 15-0 bits 15-0 H TI bi in	ost Raw Mennese bits are of the specify the terface.	nory Access Addr only used for raw 32-bit memory ac	ess bits [31:0] memory access ldress used for r	es (REG[010- aw memory a	[h] bits 1-0 = ccesses by th	01b). These e host memo
REG[0148h) Default = 00] Host Raw M 00h	lemory Acce	ess Count Regist	er 0			Read/Write
15	14	13	12	11	10	9	8
			Host Raw Memory A	ccess Count bits 7-0			
7	6	5	4	3	2	0	0
REG[014Ah Default = 00] Host Raw N 00h	lemory Acce	ess 16-bit Acces	s Count Regist	er 1		Read/Write
45	1	1 10	Host Raw Memory Ac	cess Count bits 31-24	10	0	
15	14	13	12 Host Raw Memory Ac	11 cess Count hits 23-16	10	9	8
7	6	5		2	2	0	
EG[014Ah] EG[0148h]] bits 15-0 bits 15-0 H TI bi	ost Raw Men hese bits are o ts specify the the host men	nory Access Coun only used for raw number of 16-bit mory interface du	at bits [31:0] memory accesses accesses that wi ring burst opera	es (REG[0104 ill be performe tions.	4h] bits 1-0 = ed for raw me	01b). These emory access

EPSON

REG[014Ch] Default = 000	Packed Pixe)0h	l Rectangular	X-Start Regis	ter			Read/Write	
	n/a			Packed Pixel R	ectangular X-Start P	osition bits 12-8		
15	14	13	12	11	10	9	8	
Packed Pixel Rectangular X-Start Position bits 7-0								
7	6	5	4	3	2	0	0	

bits 12-0

Packed Pixel Rectangular X-Start Position bits [12:0]

These bits are only used for packed pixel accesses (REG[0104h] bits 1-0 = 00b). These bits specify the X-Start position of the image write, in pixels, relative to the top left corner of the display area. For further information, see Section 11.1, "Display Memory Area Setup" on page 150.

REG[014Eh] Default = 000	Packed Pixel	Rectangular	Y-Start Regis	ter			Read/Write
	n/a			Packed Pixel R	ectangular Y-Start Po	sition bits 12-8	
15	14	13	12	11	10	9	8
		Pack	ked Pixel Rectangula	r Y-Start Position bit	s 7-0		
7	6	5	4	3	2	0	0

bits 12-0

Packed Pixel Rectangular Y-Start Position bits [12:0]

These bits are only used for packed pixel accesses (REG[0104h] bits 1-0 = 00b). These bits specify the Y-Start position of the image write, in pixels, relative to the top left corner of the display area. For further information, see Section 11.1, "Display Memory Area Setup" on page 150.

REG[0150h] Default = 000	REG[0150h] Packed Pixel Rectangular Width Register Default = 0000h Read/Write									
	n/a			Packed Pix	kel Rectangular Widt	h bits 12-8				
15	14	13	12	11	10	9	8			
			Packed Pixel Rectar	ngular Width bits 7-0						
7	6	5	4	3	2	0	0			

bits 12-0 Packed Pixel Rectangular Width bits [12:0]

These bits are only used for packed pixel accesses (REG[0104h] bits 1-0 = 00b). These bits specify the width of the image write, in pixels. For further information, see Section 11.1, "Display Memory Area Setup" on page 150.

REG[0152h] Default = 000	Packed Pixel	Rectangular	Height Regist	er			Read/Write
	n/a Packed Pixel Rectangular Height bits 12-8						
15	14	13	12	11	10	9	8
Packed Pixel Rectangular Height bits 7-0							
7	6	5	4	3	2	0	0

bits 12-0

Packed Pixel Rectangular Height bits [12:0]

These bits are only used for packed pixel accesses (REG[0104h] bits 1-0 = 00b). These bits specify the height of the image write, in pixels. For further information, see Section 11.1, "Display Memory Area Setup" on page 150.

REG[0154h] Default = 000	Host Memory Oh	Access Por	t Register				Read/Write
			Host Memory Ac	cess Port bits 15-8			
15	14	13	12	11	10	9	8
	•		Host Memory Ac	ccess Port bits 7-0			•
7	6	5	4	3	2	0	0
REG[0156h] Default = 000	Host Memory Oh	Checksum	Register			<u> </u>	Read/Write
			Host Memory Ch	necksum bits 15-8			
15	14	13	12	11	10	9	8
		•	Host Memory C	hecksum bits 7-0			•
7	6	5	4	3	2	0	0
bits 15-0	Hos	at Memory Cl	hecksum bits [1	5:0]		\mathcal{O}	

These bits contain a checksum value of all 16-bit memory accesses. After each 16-bit memory access, the data value is added to the value in this register.

To reset the checksum calculation, the Host must write 00h to these bits.

10.3.6 SPI Flash Memory Interface

Read OnlyRead Only15Read Only15141312111098SPI Flash Read Data bits 7-0765432107654321076543210SPI Flash Read Data bits [7:0] (Read Only) These bits contain the 8-bit data value received from the SPI Flash Memory: A read data transfer is triggered by a "dummy" write to REG[0202h] where bit 8 = 0b.REG[0202h] SPI Flash Write Data Register Default = 0000hWrite OnlyN'aSPI Flash Write Data Register Output EnableN'aSPI Flash Write Data Register Default = 0000hN'aSPI Flash Write Data Register Output EnableN'aSPI Flash Write Data Register Output EnableN'aSPI Flash Write Data Register Output EnableSPI Flash Write Data Register Output EnableYi flash Data Output Enable (Write Only)This bit determines whether a read or write data transfer takes place on the SPI Flash Memory interface. When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer from the SPI Flash Memory takes place. The read data transfer from the SPI Flash Memory takes place. The read data transfer target to improve the output for the DEC(0200h)	REG[0200h]	SPI Flash	Read Data Reg	lister								
15141312111098SPI Flash Read Data bits 7.07654321076543210poits 7-0SPI Flash Read Data bits [7:0] (Read Only) These bits contain the 8-bit data value received from the SPI Flash Memory. A read data transfer is triggered by a "dummy" write to REG[0202h] where bit 8 = 0b.n/aSPI Flash Write Data Register Default = 0000hN/aSPI Flash Write Data Register Output EnableN/aSPI Flash Write Data RegisterOutput EnableN/aSPI Flash Data RegisterOutput EnableOutput Enable15141312111098SPI Flash Write Data RegisterOutput Enable151413121110983021098SPI Flash Write Data bits 7-076543210SPI Flash Data Output Enable (Write Only)This bit determines whether a read or write data transfer takes place on the SPI Flash Memory interface. When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer from the SPI Flash Memory takes place. The read data transfer from the SPI Flash Memory takes place. The read data transfe	Default = 000	00h						Read Only				
15 14 13 12 11 10 9 8 SPI Flash Read Data bits 7-0 7 6 5 4 3 2 1 0 pits 7-0 SPI Flash Read Data bits [7:0] (Read Only) These bits contain the 8-bit data value received from the SPI Flash Memory. A read data transfer is triggered by a "dummy" write to REG[0202h] where bit 8 = 0b. A read data transfer is triggered by a "dummy" write to REG[0202h] where bit 8 = 0b. REG[0202h] SPI Flash Write Data Register Default = 0000h Write Only SPI Flash Write Data Register Default = 0000h SPI Flash Write Data Register 015 14 13 12 11 10 9 8 SPI Flash Write Data Register 015 14 13 12 11 10 9 8 SPI Flash Write Data bits 7-0 7 6 5 4 3 2 1 0 SPI Flash Data Output Enable (Write Data bits 7-0 7 6 5 4 3 2 1 0 SPI Flash Data Output Enable (Writ	n/a											
Pilash Read Data bits 7-0 7 6 5 4 3 2 1 0 Dits 7-0 SPI Flash Read Data bits [7:0] (Read Only) These bits contain the 8-bit data value received from the SPI Flash Memory. A read data transfer is triggered by a "dummy" write to REG[0202h] where bit 8 = 0b. A read data transfer is triggered by a "dummy" write to REG[0202h] where bit 8 = 0b. REG[0202h] SPI Flash Write Data Register Default = 0000h Write Only SPI Flash Data Output Enable 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 SPI Flash Write Data Output Enable (Write Only) 7 6 5 4 3 2 1 0 SPI Flash Write Data Output Enable (Write Only) This bit determines whether a read or write data transfer takes place on the SPI Flash Memory interface. When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer is triggered by a "dumm" write to REG[02020h]	15	14	13	12	11	10	9	8				
76543210bits 7-0SPI Flash Read Data bits [7:0] (Read Only) These bits contain the 8-bit data value received from the SPI Flash Memory. A read data transfer is triggered by a "dummy" write to REG[0202h] where bit $8 = 0b$. REG[0202h] SPI Flash Write Data Register Default = 0000hN/aSPI Flash Write Data RegisterDefault = 0000hWrite OnlySPI Flash Write Data RegisterOutput EnableSPI Flash Write Data RegisterOutput EnableSPI Flash Write Data RegisterOutput Enable1514131215141312SPI Flash Write Data bits 7-0765432SPI Flash Data Output Enable (Write Only) This bit determines whether a read or write data transfer takes place on the SPI Flash Memory interface. When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer is is triggered by a "dummy" write to REG[0200h]				SPI Flash Read Data bits 7-0								
bits 7-0 SPI Flash Read Data bits [7:0] (Read Only) These bits contain the 8-bit data value received from the SPI Flash Memory: A read data transfer is triggered by a "dummy" write to REG[0202h] where bit 8 = 0b. REG[0202h] SPI Flash Write Data Register Default = 0000h N/a 15 14 13 12 11 10 9 SPI Flash Data Output Enable SPI Flash Write Data bits 7-0 7 6 SPI Flash Data Output Enable (Write Only) This bit determines whether a read or write data transfer takes place on the SPI Flash Memory interface. When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer is triggered by a "dummy" write to REG[0202h]	7	6	5	4	3	2	1	0				
These bits contain the 8-bit data value received from the SPI Flash Memory: A read data transfer is triggered by a "dummy" write to REG[0202h] where bit $\$ = 0b$. REG[0202h] SPI Flash Write Data Register Default = 0000hMyrite OnlyImage: SPI Flash Write Data RegisterOutput EnableImage: SPI Flash Write Data RegisterOutput EnableSPI Flash Write Data Bits 7-0This bit determines whether a read or write Data transfer takes place on the SPI Flash Memory interface.When this bit determines whether a read or write data transfer takes place on the SPI Flash Memory takes place. The read data transfer from the SPI Flash Memory takes place. The read data transfer takes place to the SPI Flash Memory takes place. The read data transfer takes place to the SPI Flash Memory takes place. The read data transfer takes place to the SPI Flash Memory takes place.	bits 7-0		SPI Flash Read	Data bits [7:0] (l	Read Only)							
transfer is triggered by a "dummy" write to REG[0202h] where bit 8 = 0b.REG[0202h] SPI Flash Write Data RegisterDefault = 0000hN/a15141314131211109SPI Flash Write Data bits 7-0765765765Flash Write Data bits 7-076543210SPI Flash Write Data bits 7-07654320SPI Flash Data Output Enable (Write Only)This bit determines whether a read or write data transfer takes place on the SPI Flash Memory interface. When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer is triagraph by a "dummy" units to REGI0202hl			These bits conta	in the 8-bit data	value received	l from the SPI	Flash Memory	A rea <mark>d d</mark> ata				
REG[0202h] SPI Flash Write Data RegisterDefault = 0000h n/a SPI Flash Data Output Enable15141312111098SPI Flash Write Data bits 7-076543210oit 8SPI Flash Data Output Enable (Write Only) This bit determines whether a read or write data transfer takes place on the SPI Flash Memory interface. When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer is triaggored by a "dummy" write to PEC[0202h]			transfer is trigge	red by a "dumm	y" write to RE	G[0202h] who	ere bit <mark>8 = 0b.</mark>					
REG[0202h] SPI Flash Write Data Register Write Only SPI Flash Data Register N/a SPI Flash Data 15 14 SPI Flash Data SPI Flash Write Data bits 7-0 7 6 5 4 3 2 1 0 SPI Flash Write Data bits 7-0 7 6 5 4 3 2 1 0 oit 8 SPI Flash Data Output Enable (Write Only) This bit determines whether a read or write data transfer takes place on the SPI Flash Memory interface. When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer is triaggrand by a "dummy" write to REC[0202h]												
REGIOZOZIJ SPI Flash Write Data RegisterWrite OnlyN/aSPI Flash Data Output Enable15141312111098SPI Flash Write Data bits 7-076543210Output Enable (Write Data bits 7-076543210Default = 0SPI Flash Data Output Enable (Write Only)This bit determines whether a read or write data transfer takes place on the SPI Flash Memory interface.When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer is triangread by a "dummy" write to PECI0202bl												
n/a SPI Flash Data Output Enable 15 14 13 12 11 10 9 8 SPI Flash Write Data bits 7-0 7 6 5 4 3 2 1 0 other colspan="4">SPI Flash Write Data bits 7-0 7 6 5 4 3 2 1 0 other colspan="4">SPI Flash Data Output Enable (Write Only) This bit determines whether a read or write data transfer takes place on the SPI Flash Memory interface. When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer is triggered by a "dummy" write to PECI0202hl	Default = 000	oh in the second	i write Data Reg	lister				Write Only				
15 14 13 12 11 10 9 8 SPI Flash Write Data bits 7-0 7 6 5 4 3 2 1 0 5 4 3 2 1 0 bit 8 SPI Flash Data Output Enable (Write Only) This bit determines whether a read or write data transfer takes place on the SPI Flash Memory interface. When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer is triggered by a "dummy" write to PECI0202bl	n/a SPI Out											
SPI Flash Write Data bits 7-0 7 6 5 4 3 2 1 0 oit 8 SPI Flash Data Output Enable (Write Only) This bit determines whether a read or write data transfer takes place on the SPI Flash Memory interface. Memory interface. When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer is triggered by a "dummy" write to PECI0202bl	15	14	13	12	11	10	9	8				
7 6 5 4 3 2 1 0 bit 8 SPI Flash Data Output Enable (Write Only) This bit determines whether a read or write data transfer takes place on the SPI Flash Memory interface. Memory interface. When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer is triggered by a "dumm" write to PECI0202hl			i	SPI Flash Writ	e Data bits 7-0	i.						
bit 8 SPI Flash Data Output Enable (Write Only) This bit determines whether a read or write data transfer takes place on the SPI Flash Memory interface. When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer is triaggread by a "dummy" write to REC[0202b]	7	6	5	4	3	2	1	0				
This bit determines whether a read or write data transfer takes place on the SPI Flash Memory interface. When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer is triggered by a "dummy" write to REGIO202bl	bit 8		SPI Flash Data	Output Enable (V	Vrite Only)							
Memory interface. When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read			This bit determine	nes whether a re	ad or write dat	a transfer take	s place on the	SPI Flash				
When this bit = 0b, a read data transfer from the SPI Flash Memory takes place. The read data transfer is triggered by a "dummy" write to $PEG[0202h]$			Memory interfac	ce.			I					
data transfer is triggered by a "dummy" write to $\mathbf{PEG}[0202h]$			When this bit =	0b a read data ti	ansfer from th	e SPI Flash M	lemory takes n	lace. The read				
	data transfer is triggered by a "dummy" write to REG[0202b]											
When this bit $= 1b_{10}$ write data transfer to the SDL Flash Memory takes place			When this hit -	1b a write data	ransfer to the	SPLFlash Mar	j. norv takas nla	20				
when this of = 10, a write data transfer to the SFTT hash wellory takes place.			when this on -	10, a white data	indister to the		nory takes play					
oits 7-0 SPI Flash Write Data <mark>bi</mark> ts [7:0] (Write Only) 🔨 📏	bits 7-0		SPI Flash Write	Data bits [7:0] (Write Only) 🗸							
These bits are the write data register for the SPI Flash Memory. A write data transfer is			These bits are th	e write data regi	ster for the SP	I Flash Memo	ry. A write dat	a transfer is				
triggered by a write to REG[0202h] where bit $8 = 1b$. When the status flag for this register			triggered by a w	rite to REG[0202	2h] whe <mark>re</mark> bit 8	s = 1b. When the	he status flag f	or this register				
shows empty, the CPU is permitted to write data into this register.			shows empty. th	e CPU is permit	ted to write day	ta into this reg	ister.	C				
			······································									

REG[0204h] Default = 000	REG[0204h] SPI Flash Control Register Default = 0000h Read/Write								
n/a									
15	14	13	12	11	10	9	8		
SPI Flash Access Mode Select	SPI Flash Read Command Select	SPI Flas	SPI Flash Clock Divide Select bits 2-0			SPI Flash Clock Polarity Select	SPI Flash Enable		
7	6	5	4	3	2	1	0		

bit 7

SPI Flash Access Mode Select

This bit selects between Display Engine access mode and Host Register access mode. This bit must be set to 1b before performing a Display Engine operation to allow the Display Engine to communicate with SPI Flash Memory.

When this bit = 0b, Host Register access mode is selected.

When this bit = 1b, Display Engine access mode is selected.

bit 6	SPI Flash Read Command Select
	This bit selects which serial flash command is used for reading data and depends on the
	SPI Flash Memory device. Please refer to the device data sheet to determine which setting
	is appropriate.
	When this bit = $0b$, the serial flash read speed is Low.
	When this bit = 1b, the serial flash read speed is High.
bits 5-3	SPI Flash Clock Divide Select bits [2:0]
	These bits select the divide ratio for the SPI Flash Clock which is derived from either the
	PLL output or CLKI depending on the setting of the PLL Bypass Mode Enable bit,
	REG[0016h] bit 0. For further details on the clock structure, see Section Chapter 7,
	"Clocks" on page 45.

Table 10-18: SP	Flash (Clock Divide	Ratio	Selection
10000 10 10.01	1 100511	croch Diritic	1.00000	Selection

REG[0204h] bits 5-3	SPI Flash Clock Divide Ratio	REG[0204h] bits 5-3 SPI Flash Clock Divide Ratio
000b	1:2	100b 1:6
001b	1:3	101b 1:7
010b	1:4	110b 1:8
011b	1:5	111 <u>b</u> 1:9

bit 2 SPI Flash Clock Phase Select

This bit selects the SPI Flash clock phase. For a summary of the SPI Flash Memory clock phase and polarity settings, see Table 10-19 "SPI Flash Clock Phase and Polarity," on page 100.

bit 1 SPI Flash Clock Polarity Select (CPOL)

This bit selects the SPI Flash clock polarity. The following table summarizes the SPI Flash clock polarity and phase settings.

Table 10-19 : SPI Flash Clock	Ph <mark>a</mark> se	and P	olarity
-------------------------------	----------------------	-------	---------

REG[0204h] bit 2	REG[0204h] bit 1	Val <mark>id</mark> Data	Clock Idling Status
05	Ob	Rising edge of SPI Flash Clock	Low
00	1b	Fallin <mark>g e</mark> dge of SPI Flash Clock	High
16	0b	Falling edge of SPI Flash Clock	Low
	1b	Rising edge of SPI Flash Clock	High

bit 0

SPI Flash Enable

This bit controls the SPI Flash Memory interface logic. When this bit = 0b, the SPI Flash Memory interface is disabled. When this bit = 1b, the SPI Flash Memory interface is enabled.

Note

The SPI Flash Memory interface should be disabled (REG[0204h] bit 0 = 0b) before programming the SPI Flash registers, REG[0200h] ~ REG[0208h].

REG[0206h] Default = 00] SPI Flash S i <mark>04</mark> h	tatus Register					Read Only
			n	/a			
15	14	13	12	11	10	9	8
		n/a		SPI Flash Busy Flag	SPI Flash Write Data Register Empty Flag	SPI Flash Read Data Overrun Flag	SPI Flash Read Data Ready Flag
7	6	5	4	3	2	1	0
bit 3	SF Tř W W	PI Flash Busy F his bit indicates Then this bit = 0 Then this bit = 1	lag (Read Only the status of th b, the SPI Flasl b, the SPI Flasl	r) e SPI Flash M n Memory inte n Memory inte	emory interfac rface is not bu rface is busy.	e. sy (idle).	\Diamond
bit 2	SF Tł oc W W	PI Flash Write E nis bit indicates cours when data then this bit $= 0$ then this bit $= 1$	Data Register E when the SPI I written to the r b, the SPI Flash b, the SPI Flash write data to th	mpty Flag (Re Flash Write Da register is latch n Write Data re n Write Data re ne SPI Flash W	ad Only) ita register (RE ned for serializ egister is not en egister is empty /rite Data regis	G[0202h]) is a ation/transmis npty. y. (default)	empty which sion.
	10	o clear uns mag,	write data to ti	le SFI Flash w	me Data legis	REG[020]	211].
bit 1	SF Tř (R ne W W	PI Flash Read D nis bit indicates EG[0200h]) be we data is loaded then this bit = 0 then this bit = 1 o clear this flag,	bata Overrun Fl when new data fore the existin d). In this case, b, a SPI Flash I b, a SPI Flash I read the SPI F	ag (Read Only i is loaded into g data has bee the old data is Read Data ove Read Data ove lash Read Data	the SPI Flash n read (REG[0 no longer ava rrun has not oc rrun has occurr a register, REC	Read Data reg 206h] bit 0 = ilable and mus ccurred. red. 6[0200h].	gister 1b while the st be re-read.
bit 0	SF Th SF W W To	PI Flash Read D his bit indicates PI Flash Read D then this bit $= 0$ then this bit $= 1$ to clear this flag,	ata Ready Flag when read data lata register, RI b, the SPI Flas b, the SPI Flas read the SPI F	g (Read Only) from the SPL G[0200h]. n Memory reac n Memory reac lash Read Data	Flash Memory I data is not rea I data is ready. a register, REC	is available (c ady. 5[0200h].	or ready) in the

REG[0208h] Default = 000	SPI Flash (00h	Chip S	elect C	ontro	l Register					Read/Write
					I	n/a				
15	14		13		12		11	10	9	8
	n/a									SPI Flash Chip Select Enable
7	6		5		4		3	2	1	0
bit 0	S	PI Flas	sh Chip	Selec	t Enable					

This bit controls chip select (SPIDCS_L) for the SPI Flash Memory interface and is used to access the serial EEPROM.

When this bit = 0b, the chip select for the slave device is disabled. When this bit = 1b, the chip select for the slave device is enabled.

Note

The chip select output pin for the Serial Flash Memory interface is active low. Therefore, SPIDCS_L is high when this bit = 0b, and SPIDCS_L is low when this bit = 1b.

10.3.7 I2C Thermal Sensor Interface Registers

REG[0210h] Default = 000	REG[0210h] I2C Thermal Sensor Configuration Register Default = 0000h Read/Write								
n/a						I2C Thermal Sensor ID Address bits 2-0			
15	14	13	12	11	10	9	8		
			n	/a					
7	6	5	4	3	2	1	0		

bits 10-8

I2C Thermal Sensor ID Address bits [2:0]

These bits are the three least significant bits of the I2C thermal sensor ID address, A[2:0]. A[6:3] are fixed to a value of 1001b. The default value for A[2:0] is 000b, resulting in a default ID address of 100_1000b (48h).

REG Defa	REG[0212h] I2C Thermal Sensor Status Register Default = 0006h									
				n	/a					
	15	14	13	12	11	10	9	8		
	n	ı/a	I2C SDA Pin Status	I2C SCL Pin Status	n/a	I2C Thermal Sensor Data Status	I2C Thermal Sensor ID Status	I2C Thermal Sensor Busy Status		
	7	6	5	4	3	2	1	0		
bit 5		I2C Thi The Wh Wh	SDA Pin Statu s bit indicates to rmal Sensor. en this bit = 0b en this bit = 1b	us (Read Only he status of th , the I2C SDA) e I2C SDA pir pin is low (0) pin is high (1	i which is used	l to communic	ate with the		
bit 4	 I2C SCL Pin Status (Read Only) This bit indicates the status of the I2C SCL pin which is used to communicate with th Thermal Sensor. When this bit = 0b, the I2C SCL pin is low (0). When this bit = 1b, the I2C SCL pin is high (1). 							ate with the		
bit 2	 I2C Thermal Sensor Data Status (Read Only) This bit indicates the status of temperature value data returned from the Thermal Sensor. When this bit = 0b, temperature value data has been returned from the thermal sensor (ACK). When this bit = 1b, temperature value data has not been returned from the thermal sensor (NACK). 									
bit 1		I2C This Wh Wh	I2C Thermal Sensor ID Status (Read Only) This bit indicates the status of the Thermal Sensor ID transfer. When this bit = 0b, the thermal sensor ID has been transferred (ACK). When this bit = 1b, the thermal sensor ID has not been transferred (NACK).							
bit 0		I2C Thi Wh Wh	Thermal Sense s bit indicates t en this bit = 0b en this bit = 1b	or Busy Status he status of th o, the I2C thern o, the I2C thern	s (Read Only) e I2C Thermal nal sensor is ic nal sensor is b	Sensor. lle (not busy). usy.				

REG[021	4h] I2C	Therma	I Sensor Read	Trigger Regist	ter				
Default =	0007h							Write Only	
	n/a								
15		14	13	12	11	10	9	8	
				n/a				I2C Thermal Sensor Read Trigger	
7		6	5	4	3	2	1	0	
	This bit triggers the thermal sensor to read the current temperature which is stored in the I2C Thermal Sensor Temperature Value register, REG[0216h]. Writing a 0b to this bit has no effect. Writing a 1b to this bit triggers a temperature read from the Thermal Sensor.								
REG[021	6h] I2C	Therma	I Sensor Temp	erature Value	Register				
Default =	0007h							Read Only	
				n,	'a				
15		14	13	12	11	10	9	8	
1			120	C Thermal Sensor Ter	nperature Value bits	7-0			

4

bits 7-0

6

5

I2C Thermal Sensor Temperature Value bits [7:0] (Read Only) These bits indicate the temperature value received from the I2C Thermal Sensor after a I2C thermal sensor read has been triggered, REG[0214h] bit 0 = 1b. The temperature value is stored in 2's compliment format.

2

3

1

0

10.3.8 3-Wire Chip Interface Registers

REG[0220h] Default = 000	3-Wire Chip C	onfiguration	Register				Read/Write
	-		n/a				3-Wire Chip
15	14	13	12	11	10	9	8 Read/write Select
	n/a			3-Wire Chip Ir	nterface Clock Divide	Select bits 4-0	
7	6	5	4	3	2	1	0
bit 8	3-W This read bits Who Who	ire Chip Read bit selects wh write operation 7-0. en this bit = 01 en this bit = 11	l/Write Select nether a read o on is triggered o, a write oper o, a read opera	r write operati by a write to t ation is selecte tion is selected	on is performed the 3-Wire Chij ed (see REG[022	d from/to the s p Address bits 24h] bits 15-8 26h] bits 7-0).	3-Wire chip. A , REG[0224h])).
bits 4-0	3-W The The PLL ture	Tire Chip Inter se bits select t clock is deriv Bypass Mode , see Section C Table 10-20: 3	face Clock Di he divide ratio ed from either e Enable bit, R Chapter 7, "Clo -Wire Chip In	vide Select bits o used to gener the PLL outpu EG[0016h] bi ocks" on page terface Clock J	s [4:0] ate the clock fo ut or CLKI dep t 0. For further 45. Divide Selection	or the 3-Wire (ending on the details on the n	Chip interface. setting of the clock struc-
		REG[020	0h] bits 4-0	Divide	Ratio		
		0_000	0b (00h)	1:	:2		
		0_000	1b (01h)	1	:4		
		0_001	0b (<mark>0</mark> 2h) 💦 🔨	1:	:8		
		0_001	1b (0 <mark>3h)</mark>	1	16		
		0_0100b (04h	~ 1_1111b ~ 1Fh)	Rese	erved		
REGI0222h1	3-Wire Chin A	ccess Status	Register				
Default = 000	Oh		lingiotor				Read Only
15	14	13	r 12	1/a 11	10	9	8
		n/a			3-Wire Chip Data Byte Transfer Status	3-Wire Chip Address Byte Send Status	3-Wire Chip Operation Status
7	6	5	4	3	2	1	0
bit 2 bit 1	3-W This inte Who 3-W This face Who Who	Fire Chip Data bit indicates frace. en this bit = 01 en this bit = 11 fire Chip Addu bit indicates bit indicates en this bit = 01 en this bit = 11	Byte Transfer the status of th o, a data byte i o, a data byte i ress Byte Send the status of th o, an address b	• Status (Read on the data byte transfers s not being transfers being transfers l Status (Read on the address byte byte is not being transfers	Only) unsfer (send/rec nsferred (not be erred (busy). Only) e transfer (send) ug transferred (r ansferred (busy)	eive) on the 3 usy).) on the 3-Wir not busy).	-Wire Chip e Chip inter-

bit 03-Wire Chip Operation Status (Read Only)
This bit indicates the status of the 3-wire chip interface.
When this bit = 0b, the 3-wire chip interface is idle (not busy).
When this bit = 1b, the 3-wire chip interface is busy.

	000h	· - ·				- J				Re	ad/Write
					3-Wire Chip Writ	e Data bits 7-0					
15		14	13		12	11	10		9		8
7	I	6	I 6	i	3-Wire Chip Ad	dress bits 7-0	0	1	4	i.	0
		0			-	0	2				Ŭ,
its 15-8		3- Th (R	Wire Chip V ese bits spe EG[0220h]	Write D cify the bit 8 =	ata bits [7:0] e data to be v 0b). These l] written to the 3 bits are not use	3-Wire Chi ed if a read	p durin operat	ig a writ	te opera	ation
to 7 0		2 1	Wine Chin	Adamaa	hita [7.0]						
Its 7-0		ე- უს	wire Chip A	Address	DIUS [7:0]	the transfor to	or from t	2 2 1	iro Chir	A tro	nafaria
		11. tri	agered by a	write t	o these bits	the transfer to	o nom u	10 3- W	ne Cinț). A ua	lister is
		uı	geneu by a	white t	o mese ons.						
REG[0226	n] 3-W	ire Chip	Read Data	Byte F	Register			-			
Default = 0	000h	-		-	-					R	ead Onl
					n/a	a					
15		14	13		12	11	10		9		8
_	1			Т	3-Wire Chip Rea	d Data bits 7-0		1		1	
1		6	5		4	3	2		1		0
its 7-0		3-1	Wire Chip I	Read Da	ata bits [7:0]	(Read Only)					
		Th	lese bits ret	urn the	data read fro	m the 3-Wire	Chip in th	e previ	ous read	l opera	tion
		(R	EG[0220h]	bit 8 =	1b).						
		,									
)				
)				
)				
)				
)				
)				
)				
)				
)				

10.3.9 Power Pin Control Configuration Registers

Power Pin control uses the PWR[3:0] pins which can be programmed to perform a power-on/off cycle using the Power Pin Timing Delay registers (REG[0234h] ~ REG[0238h]) and the PWRCOM pin which is controlled by the Display Engine. Both PWR[3:0] and PWRCOM can be manually controlled using the bypass option (see REG[0232h]).

n/a			PWR3 Pin Status	PWR2 Pin Status	PWR1 Pin Status	PWR0 Pin Status	PWRCOM Pir		
15 14		13	(RO) 12	(RO) 11	(RO) 10	9	Status (RO)		
Power Cycle Busy (RO)			n/a	I		Power-Off Cycle Trigger (WO)	Power-On Cyc Trigger (WO)		
7	6	5	4	3	2	1	0		
oits 12-9	PV Th WI WI	PWR[3:0] Pin Status (Read Only) These bits indicates the status of the individual PWR[3:0] pins. When this bit = 0b, the PWR[3:0] pin is low (0). When this bit = 1b, the PWR[3:0] pin is high (1)							
bit 8	t 8 PWRCOM Pin Status (Read Only) This bit indicates the status of the PWRCOM pin. When this bit = 0b, the PWRCOM pin is low (0). When this bit = 1b, the PWRCOM pin is high (1).								
pit 7	Po Th WI WI	wer Cycle Busy his bit indicates hen this bit = 0t hen this bit = 1t	y (Read Only) whether a power-on/off cycle is currently happening. b, a power-on/off cycle is not happening (not busy). b, a power-on/off cycle is happening (busy).						
pit 1	Po Th cyo reg Wi Wi	Power-Off Cycle Trigger (Write Only) This bit triggers a power-off cycle on the PWR[3:0] pins. Before triggering a power-off cycle, the power pin delay times should be configured using the Power Pin Timing Dela registers, REG[0234h] ~ REG[0238h]. Writing a 0b to this bit has no effect. Writing a 1b to this bit triggers a a power-off cycle on the PWR[3:0] pins.							
oit 0	Po Th cya reg Wu Wu	wer-On Cycle 7 is bit triggers a cle, the power p gisters, REG[02 riting a 0b to thi	Frigger (Write power-on cycl in delay times 34h] ~ REG[0 is bit has no eff	Only) le on the PWR should be con 238h]. fect.	[3:0] pins. Bef figured using t	ore triggering he Power Pin	a power-on Timing Dela		

Default =	= 000	0h			CAISICI				Read/Write	
		n/a			PWR3 Pin Bypass Enable	PWR2 Pin Bypass Enable	PWR1 Pin Bypass Enable	PWR0 Pin Bypass Enable	PWRCOM Pin Bypass Enable	
15		14	1	13	12	11	10	9	8	
		n/a			PWR3 Pin Bypass Value	PWR2 Pin Bypass Value	PWR1 Pin Bypass Value	PWR0 Pin Bypass Value	PWRCOM Pin Bypass Value	
7		6		5	4	3	2	1	0	
oit 12			PWI This set d Timi Whe Whe	R3 Pin Bypass bit controls P irectly. When ing Delay bits on this bit = 0t on this bit = 1t yalue specified	Enable WR3 pin bypa bypass mode (REG[0234] - o, PWR3 pin b o, PWR3 pin b l by the PWR3	ass mode which is enabled, the ~ REG[0238h] ypass mode is ypass mode is 8 Pin Bypass V	h allows the P' Trigger bits (R) have no effec disabled. enabled and th alue, REG[022	WR3 pin outpu EG[0230h] bi ct. ue PWR3 pin o 32h] bit 4.	ut value to be ts 1-0) and th utput is set to	
oit 11			PWI This set d Timi Whe Whe	R2 Pin Bypass bit controls P irectly. When ing Delay bits on this bit = 0 t on this bit = 1 t value specified	Enable WR2 pin bypa bypass mode (REG[0234] p, PWR2 pin b p, PWR2 pin b l by the PWR2	ass mode which is enabled, the ~ REG[0238h] ypass mode is ypass mode is 2 Pin Bypass V	h allows the P' Trigger bits (R) have no effec disabled. enabled and th alue, REG[023	WR2 pin outpute (0230h) bit t. he PWR2 pin o (32h) bit 3.	ut value to be ts 1-0) and th output is set to	
bit 10			PWI This set d Timi Whe Whe	R1 Pin Bypass bit controls P irectly. When ing Delay bits on this bit = 0 on this bit = 1 value specified	Enable WR1 pin bypa bypass mode i (REG[0234] o, PWR1 pin b b, PWR1 pin b by the PWR1	ass mode whic is enabled, the ~ REG[0238h] ypass mode is ypass mode is l Pin Bypass V	h allows the P' Trigger bits (R) have no effec disabled. enabled and th alue, REG[023	WR1 pin outpute (EG[0230h] bit (t. (e PWR1 pin o (32h] bit 2.	ut value to be ts 1-0) and the output is set to	
oit 9			PWR0 Pin Bypass Enable This bit controls PWR0 pin bypass mode which allows the PWR0 pin output value to set directly. When bypass mode is enabled, the Trigger bits (REG[0230h] bits 1-0) and Timing Delay bits (REG[0234] ~ REG[0238h]) have no effect. When this bit = 0b, PWR0 pin bypass mode is disabled. When this bit = 1b, PWR0 pin bypass mode is enabled and the PWR0 pin output is set the value specified by the PWR0 Pin Bypass Value, REG[0232h] bit 1.							
bit 8			PWI This valu 1-0) Whe is se	COM Pin By bit controls P e to be set dire and the Timir en this bit = $0t$ en this bit = $1t$ t to the value	pass Enable WRCOM pin ectly. When by ng Delay bits (p, PWRCOM p p, PWRCOM p specified by th	bypass mode v pass mode is a REG[0234] ~ 1 bin bypass mod bin bypass mod bin bypass mod bin PWRCOM I	which allows the nabled, the Tr REG[0238h]) le is disabled. le is enabled an Pin Bypass Val	he PWRCOM igger bits (RE have no effect nd the PWRCO ue, REG[0232	pin output G[0230h] bits OM pin outpu 2h] bit 0.	
bit 4	PWR3 Pin Bypass Value When the PWR3 Pin Bypass Enable bit is set (REG[0232h] bit 12 = 1b), this bit specifies the value that is output on the PWR3 pin. When this bit = 0b, a 0 is output on the PWR3 pin (low). When this bit = 1b, a 1 is output on the PWR3 pin (high).									
-------	---									
bit 3	 PWR2 Pin Bypass Value When the PWR2 Pin Bypass Enable bit is set (REG[0232h] bit 11 = 1b), this bit specifies the value that is output on the PWR2 pin. When this bit = 0b, a 0 is output on the PWR2 pin (low). When this bit = 1b, a 1 is output on the PWR2 pin (high). 									
bit 2	 PWR1 Pin Bypass Value When the PWR1 Pin Bypass Enable bit is set (REG[0232h] bit 10 = 1b), this bit specifies the value that is output on the PWR1 pin. When this bit = 0b, a 0 is output on the PWR1 pin (low). When this bit = 1b, a 1 is output on the PWR1 pin (high). 									
bit 1	PWR0 Pin Bypass Value When the PWR0 Pin Bypass Enable bit is set (REG[0232h] bit $9 = 1b$), this bit specifies the value that is output on the PWR0 pin. When this bit = 0b, a 0 is output on the PWR0 pin (low). When this bit = 1b, a 1 is output on the PWR0 pin (high).									
bit 0	PWRCOM Pin Bypass Value When the PWRCOM Pin Bypass Enable bit is set (REG[0232h] bit 8 = 1b), this bit speci- fies the value that is output on the PWRCOM pin. When this bit = 0b, a 0 is output on the PWRCOM pin (low). When this bit = 1b, a 1 is output on the PWRCOM pin (high).									

REG[0234h] Default = 000	REG[0234h] Power Pin Timing Delay 0-1 Register Default = 0000h Read/Write											
n/a					Power Pin Timing	Delay 0-1 bits 11-8						
15	14	13	12	11	10	9	8					
			Power Pin Timing	Delay 0-1 bits 7-0								
7	6	5	4	3	2	1	0					
							<u> </u>					

bits 11-0

Power Pin Timing Delay 0-1 bits [11:0]

These bits specify the delay timing between PWR0 pin and PWR1 pin changes. For timing details, refer to Section 6.6.1, "Power Pin Transition Sequence for PWR[3:0]" on page 43. Delay time = ((REG[0234h] bits 11-0) ÷ 16) - 1

REG[0236h] Default = 000	Power Pin Tir)0h	ning Delay 1-2	2 Register				Read/Write
	n,	/a			Power Pin Timing	Delay 1-2 bits 11-8	
15	14	13	12	11	10	9	8
			Power Pin Timing	Delay 1-2 bits 7-0			
7	6	5	4	3	2	1	0

bits 11-0

Power Pin Timing Delay 1-2 bits [11:0]

These bits specify the delay timing between PWR1 pin and PWR2 pin changes. For timing details, refer to Section 6.6.1, "Power Pin Transition Sequence for PWR[3:0]" on page 43. Delay time = ((REG[0236h] bits 11-0) ÷ 16) - 1

REG[0238h]] Power Pin Ti	iming Delay 2-	3 Register				Deed
Default = 00	uun						Read/write
n/a					Power Pin Timing I	Delay 2-3 bits 11-8	
15	14	13	12	11	10	9	8
			Power Pin Timing	Delay 2-3 bits 7-0			
7	6	5	4	3	2	1	0
bits 11-0	Po	wer Pin Timing	Delay 2-3 bit	s [11:0]			

Power Pin Timing Delay 2-3 bits [11:0] These bits specify the delay timing between PWR2 pin and PWR3 pin changes. For timing details, refer to Section 6.6.1, "Power Pin Transition Sequence for PWR[3:0]" on page 43. Delay time = ((REG[0238h] bits 11-0) ÷ 16) - 1

10.3.10 Interrupt Configuration Registers

Default = 000	Oh	otatus Regis					Read/Write	
		Reserved	Host Memory Read/Write FIFC Error Interrupt Raw Status					
15	14	13	12	11	10	9	8	
SDRAM Self Refresh Enter/Exit Interrupt Raw Status	I2C Thermal Sensor Read Done Interrupt Raw Status	Power Management Controller Interrupt Raw Status	3-Wire Chip Interrupt Raw Status	GPIO Interrupt Raw Status	Host Memory Transfer Complete Interrupt Raw Status	Display Engine Interrupt Raw Status	SDRAM Initialization Complete Interrupt Raw Status	
7	6	5	4	3	2	1	0	
oit 9	Res The	erved default value	for this bit is (ıb.				
bit 8	Hos This is no REC Who Who	tt Memory Rea s bit indicates t ot masked by t G[0244h] bit 8 en this bit = 0t en this bit = 1t	d/Write FIFO he raw status o he Host Memo , a Host Memo , a Host Memo	Error Interrup of the Host Me ory Read/Write ory Read/Write ory Read/Write	t Raw Status mory Read/W FIFO Error I FIFO Error I FIFO Error I	rite FIFO Erro nterrupt Enable nterrupt has no nterrupt has of	r Interrupt and e bit, ot occurred. ccurred.	
	Тос	clear this status	s bit, write a H	o to either this	bit or REG[02	42h] bit 8.		
bit 7	SDI This not 7. Whe Whe	RAM Self Refi s bit indicates to masked by the en this bit = $0t$ en this bit = $1t$	esh Enter/Exi he raw status SDRAM Self , a SDRAM S , a SDRAM S	t Interrupt Raw of the SDRAN `Refresh Enter elf Refresh En elf Refresh En	v Status I Self Refresh /Exit Interrupt ter/Exit Interru ter/Exit Interru	Enter/Exit Inte Enable bit, R upt has not occ upt has occurre	errupt and is EG[0244h] bi curred. ed.	
	То с	clear this status	bit, write a 11	o to either this	bit or REG[02	42h] bit 7.		
bit 6	I2C Thermal Sensor Read Done Interrupt Raw Status This bit indicates the raw status of the I2C Thermal Sensor Read Done Interrupt and is no masked by the I2C Thermal Sensor Read Done Interrupt Enable bit, REG[0244h] bit 6. When this bit = 0b, an I2C Thermal Sensor Read Done Interrupt has not occurred. When this bit = 1b, an I2C Thermal Sensor Read Done Interrupt has occurred.							
		clear this status	bit, write a 11	b to either this	bit or REG[02	42h] bit 6.		
bit 5	Pow This mas Who Who	ver Manageme s bit indicates to ked by the Pow en this bit = 0b en this bit = 1b	nt Controller I he raw status wer Managemo , a Power Man , a Power Man	nterrupt Raw S of the Power N ent Controller nagement Cont nagement Cont	Status Aanagement C Interrupt Enab troller Interrup troller Interrup	ontroller Inter le bit, REG[02 t has not occu t has occurred	rupt and is no 244h] bit 5. rred.	
	То с	clear this status	bit, write a 11	o to either this	bit or REG[02	42h] bit 5.		

bit 4	3-Wire Chip Interrupt Raw Status This bit indicates the raw status of the 3-Wire Chip Interrupt and is not masked by the 3- Wire Chip Interrupt Enable bit, REG[0244h] bit 4. When this bit = 0b, a 3-Wire Chip Interrupt has not occurred. When this bit = 1b, a 3-Wire Chip Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[0242h] bit 4.
bit 3	GPIO Interrupt Raw Status This bit indicates the raw status of the GPIO Interrupt and is not masked by the GPIO Interrupt Enable bit, REG[0244h] bit 3. When this bit = 0b, a GPIO Interrupt has not occurred. When this bit = 1b, a GPIO Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[0242h] bit 3.
bit 2	Host Memory Transfer Complete Interrupt Raw Status This bit indicates the raw status of the Host Memory Transfer Complete Interrupt and is not masked by the Host Memory Transfer Complete Interrupt Enable bit, REG[0244h] bit 2. When this bit = 0b, a Host Memory Transfer Complete Interrupt has not occurred. When this bit = 1b, a Host Memory Transfer Complete Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[0242h] bit 2.
bit 1	Display Engine Interrupt Raw Status This bit indicates the raw status of the Display Engine Interrupt which occurs when one of the interrupts in REG[033Ah] or REG[033Ch] is triggered. This bit is not masked by the Display Engine Interrupt Enable bit, REG[0244h] bit 1. When this bit = 0b, a Display Engine Interrupt has not occurred. When this bit = 1b, a Display Engine Interrupt has occurred.
	To clear this status bit, clear the triggering interrupt in REG[033Ah] or REG[033Ch].
bit 0	SDRAM Initialization Complete Interrupt Raw Status This bit indicates the raw status of the SDRAM Initialization Complete Interrupt and is not masked by the SDRAM Initialization Complete Interrupt Enable bit, REG[0244h] bit
	When this bit = 0b, a SDRAM Initialization Complete Interrupt has not occurred. When this bit = 1b, a SDRAM Initialization Complete Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[0242h] bit 0.

REG[0242h] Interrupt Masked Status Register									
Default = 000	Uh						Read/Write		
	Reserved	Read/Write FIFO Error Interrupt Masked Status							
15	14	13	12	11	10	9	8		
SDRAM Self Refresh Enter/Exit Interrupt Masked Status	I2C Thermal Sensor Read Done Interrupt Masked Status	Power Management Controller Interrupt Masked Status	Host Memory Transfer Complete Interrupt Masked Status	Display Engine Interrupt Masked Status	SDRAM Initialization Complete Interrupt Masked Status				
7	6	5	4	3	2	1	0		
bit 9	Res The	erved default value	for this bit is 0	b.					
bit 8	Hos This (see Who Who To c	t Memory Rea s bit indicates t REG[0244h] en this bit = 0t en this bit = 1t clear this status	d/Write FIFO he masked sta bit 8). o, a Host Memo o, a Host Memo s bit, write a 1t	Error Interrupt tus of the Host ory Read/Write ory Read/Write to either this	t Masked Statu : Memory Read e FIFO Error I e FIFO Error I bit or REG[02	IS I/Write FIFO I Interrupt has no nterrupt has oc 40h] bit 8.	Error Interrupt ot occurred. ccurred.		
bit 7	SDI This REC Who Who To c	RAM Self Refi s bit indicates f G[0244h] bit 7 en this bit = 0t en this bit = 1t clear this status	resh Enter/Exit he masked sta). , a SDRAM S , a SDRAM S , a SDRAM S	: Interrupt Mas tus of the SDR elf Refresh En elf Refresh En o to either this	sked Status AM Self Refr ter/Exit Interru ter/Exit Interru bit or REG[02	esh Enter/Exit 1pt has not occ 1pt has occurre 40h] bit 7.	Interrupt (see curred. ed.		
bit 6	it 6I2C Thermal Sensor Read Done Interrupt Masked Status This bit indicates the masked status of the I2C Thermal Sensor Read Done Interrupt (see REG[0244h] bit 6). When this bit = 0b, an I2C Thermal Sensor Read Done Interrupt has not occurred. When this bit = 1b, an I2C Thermal Sensor Read Done Interrupt has occurred.To cherrify externs bit write a lb is still write a DECIO240h bit is constructed.								
bit 5	To clear this status bit, write a 1b to either this bit or REG[0240h] bit 6. Power Management Controller Interrupt Masked Status This bit indicates the masked status of the Power Management Controller Interrupt (see REG[0244h] bit 5). When this bit = 0b, a Power Management Controller Interrupt has not occurred. When this bit = 1b, a Power Management Controller Interrupt has occurred.								
	10 0	clear this status	s bit, write a It	to either this	bit or REG[02	40h] bit 5.			

bit 4	3-Wire Chip Interrupt Masked Status This bit indicates the masked status of the 3-Wire Chip Interrupt (see REG[0244h] bit 4). When this bit = 0b, a 3-Wire Chip Interrupt has not occurred. When this bit = 1b, a 3-Wire Chip Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[0240h] bit 4.
bit 3	GPIO Interrupt Masked Status This bit indicates the masked status of the GPIO Interrupt (see REG[0244h] bit 3). When this bit = 0b, a GPIO Interrupt has not occurred. When this bit = 1b, a GPIO Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[0240h] bit 3.
bit 2	Host Memory Transfer Complete Interrupt Masked Status This bit indicates the masked status of the Host Memory Transfer Complete Interrupt (see REG[0244h] bit 2). When this bit = 0b, a Host Memory Transfer Complete Interrupt has not occurred. When this bit = 1b, a Host Memory Transfer Complete Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[0240h] bit 2.
bit 1	Display Engine Interrupt Masked Status This bit indicates the masked status of the Display Engine Interrupt (see REG[0244h] bit 1) which occurs when one of the interrupts in REG[033Ah] or REG[033Ch] is triggered. When this bit = 0b, a Display Engine Interrupt has not occurred. When this bit = 1b, a Display Engine Interrupt has occurred.
	To clear this status bit, clear the triggering interrupt in REG[033Ah] or REG[033Ch].
bit 0	SDRAM Initialization Complete Interrupt Masked Status This bit indicates the masked status of the SDRAM Initialization Complete Interrupt (see REG[0244h] bit 0). When this bit = 0b, a SDRAM Initialization Complete Interrupt has not occurred. When this bit = 1b, a SDRAM Initialization Complete Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[0240h] bit 0.

REG[0244h] Default = 000	Interrupt Con 0h	trol Register					Read/Write			
		Reserved	Host Memory Read/Write FIFO Error Interrupt Enable							
15	14	13	12	11	10	9	8			
SDRAM Self Refresh Enter/Exit Interrupt Enable	I2C Thermal Sensor Read Done Interrupt Enable	I2C Thermal Power Sensor Read Management 3-Wire Chip GPIO Interrupt Host Memory Display Engine I Jone Interrupt Controller Interrupt Enable Interrupt Enable GPIO Interrupt Complete Interrupt Enable Interrupt Enable								
7	6	5	4	3	2	1	0			
bit 9	Reso The	erved default value	for this bit is (ıb.		\mathbf{X}				
bit 8	Hos This inter ing Who Who	t Memory Reas s bit controls w rrupt request o REG[0240h] b en this bit = 0b en this bit = 1b	d/Write FIFO whether the Ho on the HIRQ pi bit 8 (unmaske o, the interrupt o, the interrupt	Error Interrup st Memory Re n. The status of d) or REG[024 is disabled. is enabled.	t Enable ad/Write FIFO of this interrupt [2h] bit 8 (mas	Error Interrug can be detern ked).	ot causes an nined by read-			
bit 7	SDRAM Self Refresh Enter/Exit Interrupt Enable This bit controls whether the SDRAM Self Refresh Enter/Exit Interrupt causes an inter- rupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 7 (unmasked) or REG[0242h] bit 7 (masked). When this bit = 0b, the interrupt is disabled.									
bit 6	I2C This requ REC Who Who	Thermal Sens s bit controls w lest on the HIF G[0240h] bit 6 en this bit = 0t en this bit = 1b	or Read Done whether the I2C Q pin. The sta (unmasked) o o, the interrupt o, the interrupt	Interrupt Enat Thermal Sens atus of this inte r REG[0242h] is disabled. is enabled.	ble for Read Done errupt can be d bit 6 (masked	Interrupt caus etermined by 1).	es an interrupt reading			
bit 5	 it 5 it 5 Power Management Controller Interrupt Enable This bit controls whether the Power Management Controller Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 5 (unmasked) or REG[0242h] bit 5 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled. 									
bit 4	3-W This HIR (uni Who Who	Vire Chip Intens s bit controls w Q pin. The sta nasked) or RE en this bit = 0t en this bit = 1t	rupt Enable whether the 3-V itus of this inte G[0242h] bit o, the interrupt o, the interrupt	Wire Chip Inter errupt can be de 4 (masked). is disabled. is enabled.	rrupt causes an etermined by r	interrupt requ eading REG[0	lest on the 240h] bit 4			

bit 3	GPIO Interrupt Enable This bit controls whether the GPIO Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 3 (unmasked) or REG[0242h] bit 3 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 2	Host Memory Transfer Complete Interrupt Enable This bit controls whether the Host Memory Transfer Complete Interrupt causes an inter- rupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 2 (unmasked) or REG[0242h] bit 2 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 1	Display Engine Interrupt Enable This bit controls whether the Display Engine Interrupt causes an interrupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 1 (unmasked) or REG[0242h] bit 1 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 0	SDRAM Initialization Complete Interrupt Enable This bit controls whether the SDRAM Initialization Complete Interrupt causes an inter- rupt request on the HIRQ pin. The status of this interrupt can be determined by reading REG[0240h] bit 0 (unmasked) or REG[0242h] bit 0 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.

10.3.11 GPIO Control Registers

Default = 0	0000h	c conny	garation net	,				Read/Write
				n/a			GPIO1 Pull-down	GPIO0 Pull-dowr
15		14	13	12	11	10	9	8
				n/a			GPIO1 Configuration	GPIO0 Configuration
7		6	5	4	3	2	1	0
oits 9-8		Al pu W (da W	PIO[1:0] Pul Il GPIO pins ill-down resis hen the bit = efault) hen the bit =	 -down Control have internal pul stor for each GPI 0b, the pull-dow 1b, the pull-dow 	l-down resistor Ox pin. 'n resistor for th 'n resistor for th	rs. These bits c he correspondi he correspo <mark>n</mark> di	ontrol the state ng GPIOx pin ng GPIO pin is	of the is inactive. s active.
its 1-0 REG[0252	h] GPI	GI Tř W W	PIO[1:0] Connese bits contributed bits contributed bits contributed bits bit = ben this bit = ben this bit = ben this bit = ben this bits bits bits bits bits bits bits bi	figuration figure each indivi- ob, the correspo- b, the correspo- cister	dual GPIO pin onding GPIO p onding GPIO p	i between an in in is configured in is configured	put or an outp 1 as an input p 1 as an output	ut. in. (default) pin.
Default = 0	000h	e etata		5.0101				Read/Write
				n/a			GPIO1 Input Status (RO)	GPIO0 Input Status (RO)
15		14	13	12	11	10	9	8
				n/a			GPIO1 Data Output Control	GPIO0 Data Output Control
7		6	5	4	3	2	1	0
oits 9-8 oits 1-0		GI W ret W GI GI	PIO[1:0] Inp hen GPIOx i turns the stat hen this bit = hen this bit = PIO[1:0] Dat hen GPIOx i	ut Status (Read C s configured as a e of the correspon- 0b, the GPIOx p = 1b, the GPIOx p a Output Control s configured as a	only) n input (see RI nding GPIOx p pin is 0 (low). pin is 1 (high).	EG[0250h] bits bin. REG[0250h] bit	1-0), a read fr	rom this bit
		dr W W	hen this bit = hen this bit =	ut state of the correspo = 0b, the correspo = 1b, the correspo	rresponding GPIOx j onding GPIOx j	PIOx pin. pin is driven to pin is driven to	0 (low). (defa 1 (high).	ult)

			• .								
REG[0254h] Default = 000	GPIO Interrup 10h	ot Enable Reg	ister				Read/Write				
		n	/a			GPIO1 Negative Edge Interrupt Enable	GPIO0 Negative Edge Interrupt Enable				
15	14	13	12	11	10	9	8				
		n	/a			GPIO1 Positive Edge Interrupt Enable	GPIO0 Positive Edg <mark>e</mark> Interrupt Enable				
7	6	5	4	3	2	1	0				
bits 9-8	 GPIO[1:0] Negative Edge Interrupt Enable These bits control whether the corresponding GPIOx interrupt (see REG[0256h]) is trig- gered on the negative edge (when the GPIOx pin changes from 1 to 0). When this bit = 0b, the corresponding GPIOx interrupt is not triggered on the negative edge. (default) When this bit = 1b, the corresponding GPIOx interrupt is triggered on the negative edge. 										
bits 1-0	GPI The gere Wh edg Wh	O[1:0] Positives estables bits control ed on the positive en this bit = 0these (default) en this bit = 1these bits = 1these b	e Edge Interru whether the co ive edge (when o, the correspo o, the correspo	pt Enable orresponding C n the GPIOx pi nding GPIOx i nding GPIOx i	GPIOx interrup in changes from nterrupt is not nterrupt is trig	t (see REG[02 n 0 to 1). triggered on tl gered on the p	256h]) is trig- ne positive ositive edge.				

RE	REG[0256h] GPIO Interrupt Status Register												
De	efault = 0	0000h								•			Read/Write
						n/a						GPIO1 Negative Edge Interrupt Status	GPIO0 Negative Edge Interrupt Status
	15		14		13		12		11		10	9	8
						n/a						GPIO1 Positive Edge Interrupt Status	GPIO0 Positive Edge Interrupt Status
	7		6		5		4		3		2	1	0
bits	pits 9-8 GPIOI 1:01 Negative Edge Interrupt Status												

bits 9-8	GPIO[1:0] Negative Edge Inferrupt Status
	Th <mark>ese bits indicate the status of the corr</mark> esponding GPIOx Negative Edge Interrupt.
	When this bit = 0b, a Negative Edge Interrupt has not occurred. (default)
	When this bit = 1b, a Negative Edge Interrupt has occurred.
	To clear this status bit, write a 1b to this bit.
bits 1-0	GPIO[1:0] Positive Edge Interrupt Status
	These hits indicate the status of the corresponding CDIOx Desitive Edge Interrupt
	These bits indicate the status of the corresponding GPIOX Positive Edge interrupt.
	When this bit = $0b$, a Positive Edge Interrupt has not occurred. (default)
	When this bit = 1b, a Positive Edge Interrupt has occurred.
	To clear this status bit, write a 1b to this bit.

10.3.12 Command RAM Controller Registers



10.3.13 Command Sequencer Controller Registers

REG[02A0h] Command Sequencer Controller Index Register Default = 0000h Read/Write									
n/a									
15	14	13	12	11	10	9	8		
n	/a								
7	6	5	4	3	2	1	0		

bits 5-0

Command Sequencer Index Select bits [5:0]

These bits select the index for the Command Sequencer Data Port, REG[02A2h

REG[02A2h Default = 00] Command 00h	Sequencer Cor	ntroller Data F	Port Register			Read/Write
			Command Sequence	er Data Port bits 15-	8		
15	14	13	12	11	10	9	8
			Command Sequen	cer Data Port bits 7-0	0		
7	6	5	4	3	2	1	0
bits 15-0	C	Command Sequer	ncer Data Port	bits [15:0]			

bits 15-0

Command Sequencer Data Port bits [15:0]

These bits are the Command Sequencer Data Port where each Index data has the following bit configuration: bits 15-13 are the Command Parameter Number

bits 9-0 are the Command RAM Address Pointer

REG[030 Default =	0h] Fra 0000h	ime Data	a Length Reg	jister				Read/Write
		n/a				Frame Data Length b	bits 12-8	
15		14	13	12	11	10	9	8
				Frame	Data Length bits 7-0			
7		6	5	4	3	2	1	0
oits 12-0		F	rame Data Le	ength bits [12	:0]			
		Т	hese bits spec	cify the frame	data length, in l	ines.		
			Frame data	a length = RE	G[0300h] bits 12	2-0		
REG[030	2h] Fra	ime Syn	c Length Re	gister				
Default =	0000h							Read/Write
45	1		1 40	10	n/a	10		0
15		14	13	Frame	Sync Length bits 7-0	10	9	8
7		6	5	4	3	2	1	0
nits 7-0		F	rame Sync Le	enoth hits [7·()I 🧹			
511370		Т	hese hits snew	rify the frame	sync length in	lines		
		1	Frame syn	$c_{1} = (\mathbf{P})^{2}$	FG[0302b] Kite	7 0 + 1		
			Traine syn	c length – (K		-0) + 1		
						•		
REG[030	4h] Fra	me Beg	in/End Leng	th Register				
Default =	0104h	•	•					Read/Write
				Frame	End Length bits 7-0			
15		14	13	12	11	10	9	8
			I	Frame	Begin Length bits 7-0	I	1	1
7		6	5	4	3	2	1	0
oits 15-8		F	rame End Lei	ngth bits [7:0]				
		Т	hese bits spec	cify the frame	end length, in li	nes.		
			Frame end	length = RE	G[0304h] bits 15	-8		
				•				
		N	ote					
			These bits m	ust be progra	mmed such that	the following f	formula is va	lid.
			REG[03	04h] bits 15-8	$3 \ge 1$			
bite 7.0			romo Bogin I	ongth hits [7]	•01			
			hasa bita ana	wife the frame	.0] hagin langth in	lines		
		1	Frame beg	in length $=$ R	EG[0304h] bits '	7-0		
~ <i>/</i>		N	ote					
		IN	These hits m	ust he program	mmed according	to the gate driv	ver specificat	ion For the Shar
			I H1607 the	se hits must h	he set to 4h For	other generic (Tate drivers	these hits must be
			set to Ob	se ons must t	Je set to 411, 1701 (Suici generie C		mese ons must be
			set to UII.					

10.3.14 Display Engine: Display Timing Configuration

	00h										Read/Writ
	n/a						Line Dat	a Length b	its 12-8		
15	14		13		12	11 ath hite 7.0		10		9	8
7	6	1	5	I		19111 DILS 7-0 3	1	2	1	1	
								-			
ts 12-0		Line Thes	Data Leng se bits speci Line data le	fy the ngth =	= [12:0] = line data le = REG[0306	ngth, in pi 5h] bits 12	xels. -0				
		W mu bit	hen 4 pixel ultiple of 4 j ts must be s	outpu pixels et to a	it is selected . When 8 pi multiple of	(REG[03 xel output 8 pixels.	0Ch] bi is selec	t 11 = 0 cted (RE	b), the EG[030	se bits m)Ch] bit	11 = 1b), thes
EG[0308h efault = 00] Line Sy 00h	nc Ler	ngth Regist	er			•	7	Č		Read/Writ
15	14		13		n/: 12	a 11		10		9	8
7	6	1	5	I		ngth bits 7-0	1	2	1	1	0
		For 4	se bits speci lepending of 4 pixel outp Line sync le 8 pixel outp Line sync le	fy the n the j ut (R) ength ut (R) ength	E[17.8] Eline sync le pixel output EG[030Ch] $= REG[030$ $EG[030Ch]$ $= REG[030$	ength, in 4 count bit $11 = 01$ 8h] bits 7- bit $11 = 11$ 8h] bits 7-	pixel in b): 0 x 4 + b): 0 x 4 +	4 + 2) 8 + 2)	nts, and	l are offs	et by 4 or 8 p
	1 I ' D	gin/ <mark>Er</mark>	nd Len <mark>gth</mark> F	R <mark>e</mark> gis	ter						Read/Writ
EG[030A h efault = 00	00h										
EG[030Ah efault = 00 ¹⁵	00h		13		Line End Ler	igth bits 7-0 11	[10		9	8
EG[030Ah efault = 00 15	00h		13		Line End Ler 12 Line Begin Le	igth bits 7-0 11 ingth bits 7-0		10		9	8
EG[030Ah efault = 00 15 7	00h	l	<u>13</u>		Line End Ler 12 Line Begin Le 4	11 11 ngth bits 7-0 3		10 2		9	8

Line begin length = REG[030Ah] bits 7-0 x 4

EPSON

10.3.15 Display Engine: Driver Configurations

REG[030Ch] Source Driver Configuration Register Default = 0064h Read/Write									
S	ource Driver Chip B	Enable Start bits 3-0		Source Driver Pixel Output Count Select	Source Driver Chip Enable Reverse	Source Driver Output Reverse	Source Driver Shift Right		
15	14	13	12	11	10	9	8		
	Source Driver Output Size Select bits 7-0								
7	6	5	4	3	2	1	0		

bits 15-12

Source Driver Chip Enable Start bits [3:0]

These bits determine the number of the driver chip to start driving. The Source Driver Chip Enable Reverse bit (REG[030Ch] bit 10) can be used to reverse the chip enable sequence. For an example, see the following table.

Table 10-21: Example of Chip Enable Start + Chip Enable Reverse (ChipSize = 268, Line Size = 800)

REG[030Ch] bit 10	REG[030Ch] bits 15-12	Chip En <mark>able</mark> Sequence		
	0000b	C <mark>hip0 -> Chip1 -</mark> > Chip2		
Ob	0001b	C <mark>hip</mark> 1 -> Chip2 -> Chip0		
dU	0010b	Chip2 -> Chip0 -> Chip1		
	0011b ~ 1111b	Reserved		
	0000b	Chip0 -> Chip2 -> Chip1		
16	0001b	Chip1 -> Chip0 -> Chip2		
Ŭ	0010 <mark>b</mark>	Chip2 -> Chip1-> Chip0		
	0011b ~ 1111b	Reserved		

bit 11

Source Driver Pixel Output Count Select

This bit selects the number of parallel pixels output per Source Driver clock. When this bit = 0b, the source driver outputs 4 pixels per clock. When this bit = 1b, the source driver outputs 8 pixels per clock.

bit 10 Source Driver Chip Enable Reverse

This bit configures the enable sequence for multiple chip selects. The number of chip selects is determined by the Line Data Length bits (REG[0306h] bits 12-0) and the Source Driver Output Size Select bits (REG[030Ch] bits 6-0). Using these bits with the Source Driver Chip Enable Start bit provides full configurability of the count down sequence. When this bit = 0b, the source driver chip enable sequence is not reversed. When this bit = 1b, the source driver chip enable sequence is reversed.

bit 9

bit 8

Source Driver Output Reverse This bit selects the parallel pixels output arrangement.

REG[030Ch] bit 11	Pixels Arrangement in Little Endian	REG[030Ch] bit 9	Parallel Output to Source Driver
0	P3,P2,P1,P0	0	P3,P2,P1,P0
0	P3,P2,P1,P0	1	P0,P1,P2,P3
1	P7,P6,P5,P4,P3,P2,P1,P0	0	P7,P6,P5,P4,P3,P2,P1,P0
1	P7,P6,P5,P4,P3,P2,P1,P0	1	P0,P1,P2,P3,P <mark>4,</mark> P5, <mark>P6,</mark> P7

This bit determines how the source driver shifts the Serial to Parallel data.

When this bit = 0b, the serial to parallel data is shifted from Left to Right. The first data input is shifted from the last source driver output to the first source driver output (i.e. for 268 size, $268 \rightarrow 1$). This means the first data accepted by the source driver will appear on

When this bit = 1b, the serial to parallel data is shifted from Right to Left. The first data input is shifted from the first source driver output to the last source driver output (i.e. for 268 size, $1 \rightarrow 268$). This means the first data accepted by the source driver will appear on

Table 10-22:	Source L	Driver O	utnut Reverse	Function
10000 10 22.	Source L		mpm neverse	1 1111011011

bits 7-0Source Driver Output Size Select bits [7:0]These bits select the source driver output size per chip.

the first line of the source driver.

Source Driver Shift Right

REG[030Ch] bits 7-0 = value in pixels x 4 Default = 0x64 (400d)

REG[030Eb]	Gate Driver	Configuration	Register						
Default = 000	Oh	Comgulation	inegister				Read/Write		
	Source Driver SDOED Delay bits 4-0 Source Driver Double Data Rate Enable								
15	14	13	12	11	10	9	8		
	Source	e Driver SDOEX Dela		n/a	Gate Driver Right/Left Select	Gate Driver Start Pulse Polarity			
7	6	5	4	3	2	1	0		
bit 10	Son Th Son Th Wh Wh itiv	ese bits specify urce Driver Do is bit is used w nen this bit = 0 nen this bit = 1 we and negative	w the SDOED (buble Data Rate when the source b, 8 pixels are b, the data rate e edges).	SDCE_L10 pi Enable driver pixel of output per SD0 is doubled and	n) delay from s utput count is s CLK. d 4 pixels are o	SDLE, in SDC et to 8 pixels. utput per SDC	LKs. LK edge (pos-		
bit 9	Source Driver Swap Padding Pixels This bit is used in combination with the Source Driver Shift Right bit (REG[030Ch] bit 8) and causes pixels padding whenever the Source Driver chip contains extra unused/non- display pixels.								

Table 10-23: Source Driver Padding Pixels Position

REG[030Eh] bit 9	REG[030Ch] bit 8	Padding Data Location
0b	0b	Extra Pixels will be padded at the end of the Last Chip
0b	1b	Extra Pixels will be padded at the beginning of the First Chip
1b	0b	Extra Pixels will be padded at the beginning of the First Chip
1b	1b	Extra Pixels will be padded at the end of the Last Chip

bit 8	Source Driver Early SDOE Assert Disable
	This bit determines whether SDOE is asserted 1 line early before SDLE in normal opera-
	tion (for non-Micronix source drivers). This setting should be acceptable for Micronix
	source drivers also. However, if this method causes problems on Micronix source drivers,
	it can be disabled using this bit.
	When this bit = 0b, Source Driver Early SDOE Assert is enabled.
	When this bit = 1b, Source Driver Early SDOE Assert is disabled.
bits 7-3	Source Driver SDOEX Delay bits [4:0]
	These bits specify the SDOEX (SDCE_L9 pin) delay from SDLE, in SDCLKs.
bit 1	Gate Driver Right/Left Select
	This bit selects the gate driver GDRL pin output.
	When this bit = 0b, the Gate Driver GDRL pin output is left.
	When this bit = 1b, the Gate Driver GDRL pin output is right.
bit 0	Gate Driver Start Pulse Polarity
	This bit controls the gate driver start pulse polarity.
	When this bit $= 0b$, the polarity is negative.
	When this bit $= 1b$, the polarity is positive.

10.3.16 Display Engine: Memory Region Configuration Registers

REG[0310h]	Image Buf	fer Start Addre	ess Register 0				Pood/Mrito
	001						Reau/ Wille
45	1 44		Image Buffer Start A	Address bits 15-8	10		
15	14	13	12 Image Buffer Start	11 Address bits 7-0	10	9	8
7	6	5		2	2	1	
1	0	5	4	5	2	1	
REG[0312h]	Image Buf	fer Start Addre	ess Register 1				Read/Write
	0011		2/2				Address hits 25.2
45	1 14	10	n/a	44	10	image Buller Sta	
15	14	13	Image Buffer Start A	ddress bits 23-16	10	9	0
7	6	5		3	2		0
,	0	5	т	0	2		- 0
EG[0310h]	bits 15-0 I T	mage Buffer St These bits speci	art Address bits [2 fy the Image Buff	25:0] er start address	in SDRAN	I byte address	space.
REG[0314h] Default = 000	Update Bu 00h	ffer Start Addr	ess Register 0	Ś	\checkmark		Read/Write
			Update Buffer Start	Address bits 15-8			
15	14	13	12	11	10	9	8
			Update Buffer Start	Address bits 7-0			
7	6	5	4	3	2	1	0
REG[0316h] Default = 000	Update Bu)0h	ffer Start Addr	ress Register 1	\sim	X.		Read/Write
	1	1	Update Buffer Start A	ddress bits 31-24		1	1
15	14	13	12	11	10	9	8
7						1	
1	6	5	4		2	1	0
EG[0314h]	bits 15-0 L	Jpdate Buffer S These bits speci:	tart Address bits fy the Update Buf	[31:0] fer start addres	s in SDRA	M byte address	space.

10.3.17 Display Engine: Component Control

				'a			
15	1.4	13	12	11	10	0	ß
15	14	13 n/a	12		10	Temperature Device Source Select	Temperature Auto Retrieval Disable
7	6	5	4	3	2	1	0
oit 1	Te Th Se W	mperature Devic is bit selects between r_{1} models between r_{2} models $r_$	the Source Sele ween the I2C t is bit must be , the I2C therm , the Dialog D	ct hermal senso set to 0b wh nal sensor is A8590 IC is	or or the Dialog en the Dialog D selected. selected for poy	DA8590 IC fo A8590 IC is n wer manageme	r Temperatur ot present. ent.
ont O	Th 1) W	mperature Auto is bit determines on every update hen this bit = $0b$, hen this bit = $1b$,	s whether the t frame operati , temperature f	emperature i on. retrieval is er retrieval is di	s retrieved from abled. (default) sabled.	the selected d	evice (see bit
REG[0322h Default = 00] Temperature 00h	e Value Registe	r				Read/Write
			n/	a			
15	14	13	12 Tomporatura	11	10	9	8
7	6	5				1	
oits 7-0	Te Th ne bit	mperature Value tese bits store the xt display update 0 = 0b), these b	bits [7:0] temperature operation, W its are automa	value which hen Tempera tically updat	will be used for ture Auto Retric ed on every frar	Waveform ret eval is enabled ne update oper	rieval on the (REG[0320h ation.
REG[0324h Default = 00] DWELL Tim 00h	e Configuration	Register				Read/Write
15	14	13	n/ 12 Dwell Time Updat	a 11 e Interval bits 7-0	10	9	8
7	6	5	4	3	2	1	0
oits 7-0		well Time Update	e Interval bits the update inte	[7:0] ervals, in fran	nes.		

									Read/write
		1	Saved - N	lext Border Val	ue Status bits 7-	0 (RO)			
15	14	13	Na	12 # Dardar Value	11 Deguaat bita 7 (1	0	9	8
7	6	5	INEX		Request bits 7-0	, 2	>	1	۰ ۱
	~			·			<u> </u>		
oits 15-8	Sa	ved - Next I	Border V	alue Status	s bits [7:0] (Read Onl	y)		
	Th	lese bits ind	icate the	saved Nex	t Border Va	lue which	n will be	used for N	N-frame transfe
oits 7-0	Ne	ext Border V	/alue Coi	ntrol Requ	est bits [7:0	1			
	Th	ese bits spe	cify the l	Next Bord	er Value req	uested. D	ependin	g on the \mathbf{L}	UT index mod
	the	e proper MS	B bits w	ill be selec	ted for the	LUT Inde	х.		
	Denden Com	(4					
REG[0328n]	Border Coni	riguration F	kegister	1					- Pood Only
Saved Bravious	Portor Value Status							2.	iteau Oni
bite	s 1-0			n/a	a			Border D	well Time bits 1-0
15	14	13		12	11	1	0	9	8
_		1 -		Current Border	Value bits 7-0	1 .	. 1		
its 15-14	Sa	ved - Previo	ous Bord	er Value St	tatus bits [1	0] (Read	Only)		
	Th	ese hits ind	icate the	saved Cur	rent Border	Value wh	ich will	be used fo	or N-frame tran
	for		icate the	savea cui		varue wi		be used to	
	101								
	No	te				•			
	No]	te If dwell time	e LUT In	n <mark>dex M</mark> ode	is selected,	t <mark>h</mark> e Bord	er Dwel	l time valu	e is fixed to 3h
	No] (te If dwell time (Max).	e LUT Ir	ndex Mode	is selected,	the Bord	er Dwell	l time valu	e is fixed to 3h
	No] (te If dwell time (Max).	e LUT Ir	ndex Mode	is selected,	the Bord	er Dwel	l time valu	e is fixed to 3h
bits 9-8	No] (Bo	te If dwell time (Max). order Dwell	e LUT Ir T <mark>im</mark> e bit	ndex Mode	is selected,	the Bord	er Dwell	l time valu	e is fixed to 3h
oits 9-8	No] (Bc Th	te If dwell time (Max). order Dwell uese bits ind	e LUT Ir Time bit icate <mark>th</mark> e	ndex Mode s [1:0] (Re dwell time	is selected, ad Only) e for Border	the Bord updates.	er Dwel	l time valu	e is fixed to 3h
oits 9-8	No] (Bc Th Sa	te If dwell time (Max). order Dwell tese bits ind yed - Curre	e LUT In Time bit icate the	ndex Mode s [1:0] (Re dwell time	is selected, ad Only) of for Border	the Bord updates.	er Dwel	l time valu	e is fixed to 3h
oits 9-8 oits 7-0	No] (Bc Th Sa Th	te If dwell time (Max). order Dwell uese bits ind ved - Curre	e LUT Ir Time bit icate the nt Borde	ndex Mode s [1:0] (Re dwell time r Value Co saved Cur	is selected, ad Only) of for Border ntrol bits [7 rent Border	the Bord updates. :0] (Read Value wh	er Dwell	l time valu	e is fixed to 3h
oits 9-8 oits 7-0	No] (Bo Th Sa Th fer	te If dwell time (Max). order Dwell nese bits ind ved - Curre nese bits ind	e LUT Ir Time bit icate the nt Borde icate the	ndex Mode (1:0] (Re dwell time r Value Co saved Cur	is selected, ad Only) e for Border ntrol bits [7 rent Border	the Bord updates. :0] (Read Value wh	er Dwell Only) iich will	l time valu be used fo	e is fixed to 3h or N-frame tran
oits 9-8 oits 7-0	No l (Bo Th Sa Th fer	te (Max). order Dwell nese bits ind ved - Curre nese bits ind rs.	e LUT Ir. Time bit icate the nt Borde. icate the	ndex Mode s [1:0] (Re dwell time r Value Co saved Cur	is selected, ead Only) e for Border ntrol bits [7 rent Border	the Bord updates. :0] (Read Value wh	er Dwell Only) iich will	l time valu be used fo	e is fixed to 3h or N-frame tran
oits 9-8 oits 7-0	No 1 (Bo Th Sa Th fer	te (Max). order Dwell nese bits ind ved - Curre nese bits ind rs.	e LUT Ir Time bit icate the nt Borde icate the	ndex Mode as [1:0] (Re dwell time r Value Co saved Cur	is selected, ad Only) e for Border ntrol bits [7 rent Border	the Bord updates. :0] (Read Value wh	er Dwell Only) iich will	l time valu be used fo	e is fixed to 3h or N-frame tran
oits 9-8 oits 7-0	No 1 (Bo Th Sa Th fer	te (Max). order Dwell nese bits ind ved - Curre nese bits ind rs.	e LUT Ir Time bit icate the nt Borde icate the	ndex Mode s [1:0] (Re dwell time r Value Co saved Cur	is selected, ad Only) e for Border ntrol bits [7 rent Border	the Bord updates. :0] (Read Value wh	er Dwell Only) iich will	l time valu be used fo	e is fixed to 3h or N-frame tran
oits 9-8 oits 7-0	No I Bo Th Sa Th fer	te If dwell time (Max). order Dwell nese bits ind ved - Curren nese bits ind rs.	e LUT Ir Time bit icate the nt Borde icate the	ndex Mode (1:0] (Re dwell time r Value Co saved Cur	is selected, ad Only) e for Border ntrol bits [7 rent Border	the Bord updates. :0] (Read Value wh	er Dwell Only) iich will	l time valu be used fo	e is fixed to 3h or N-frame tran
oits 9-8 oits 7-0	No l (Bc Th Sa Th fer	te (Max). order Dwell nese bits ind wed - Curre: nese bits ind rs.	e LUT In Time bit icate the nt Borde icate the	ndex Mode s [1:0] (Re dwell time r Value Co saved Cur	is selected, ead Only) e for Border ntrol bits [7 rent Border	the Bord updates. :0] (Read Value wh	er Dwell Only) iich will	l time valu be used fo	e is fixed to 3h or N-frame tran
oits 9-8 oits 7-0	No 1 (Bo Th Sa Th fer	te (Max). order Dwell nese bits ind ved - Curre nese bits ind rs.	e LUT Ir Time bit icate the nt Borde icate the	ndex Mode as [1:0] (Re dwell time r Value Co saved Cur	is selected, ad Only) e for Border ntrol bits [7 rent Border	the Bord updates. :0] (Read Value wh	er Dwell Only) iich will	l time valu be used fo	e is fixed to 3h or N-frame tran
oits 9-8 oits 7-0	No l (Bo Th Sa Th fer	te (Max). order Dwell nese bits ind ved - Curren nese bits ind rs.	e LUT Ir Time bit icate the nt Borde icate the	ndex Mode ss [1:0] (Re dwell time r Value Co saved Cur	is selected, ad Only) e for Border ntrol bits [7 rent Border	the Bord updates. :0] (Read Value wh	er Dwell Only) iich will	l time valu be used fo	e is fixed to 3h or N-frame tran
oits 9-8 oits 7-0	No l (Bc Th Sa Th fer	te If dwell time (Max). order Dwell nese bits ind ved - Curren nese bits ind rs.	e LUT Ir Time bit icate the nt Borde icate the	ndex Mode s [1:0] (Re dwell time r Value Co saved Cur	is selected, ad Only) e for Border ntrol bits [7 rent Border	the Bord updates. :0] (Read Value wh	er Dwell Only) iich will	l time valu be used fo	e is fixed to 3h or N-frame tran
oits 9-8 oits 7-0	No 1 (0 Bo Th Sa Th fer	te If dwell time (Max). order Dwell nese bits ind ved - Curre nese bits ind rs.	e LUT In Time bit icate the nt Borde icate the	ndex Mode s [1:0] (Re dwell time r Value Co saved Cur	is selected, ead Only) e for Border ntrol bits [7 rent Border	the Bord updates. :0] (Read Value wh	er Dwell Only) iich will	l time valu be used fo	e is fixed to 3h or N-frame tran

REG[032Ah Default = 00) Power Contr 00Fh	ol Configurati	ion Register				Read/Write
			n/a				Voltage Control Byte Force Frame Wait
15	14	13	12	11	10	9	8
	Voltage Control Byte	e Wait Select bits 3-0)	Voltage Control Byte 3 Enable	Voltage Control Byte 2 Enable	Voltage Control Byte 1 Enable	Voltage Control Byte 0 Enable
7	6	5	4	3	2	1	0

These bits are only active when the Waveform data format is version 1 - voltage control format. This bits correspond to the Version 1 waveform data which contains an additional 4 bytes at the beginning of each temperature compensated waveform data.

bit 8	Voltage Control Byte Force Frame Wait This bit forces the number of frames specified by REG[032Ah] bits 7-4 to be skipped before the next frame is displayed.
bits 7-4	Voltage Control Byte Wait Select bits [3:0] When the value of a voltage control byte changes, these bits specify the number of frames that are skipped before the next frame is displayed.
bit 3	Voltage Control Byte 3 Enable This bit controls Power Control programming. When this bit = 0b, Voltage Control Byte 3 is disabled. When this bit = 1b, Voltage Control Byte 3 is enabled.
bit 2	Voltage Control Byte 2 Enable This bit controls Power Control VCOMS programming. When this bit = 0b, Voltage Control Byte 2 is disabled. When this bit = 1b, Voltage Control Byte 2 is enabled.
bit 1	Voltage Control Byte 1 Enable This bit controls Power Control VEES/VCCS programming. When this bit = 0b, Voltage Control Byte 1 is disabled. When this bit = 1b, Voltage Control Byte 1 is enabled.
bit 0	Voltage Control Byte 0 Enable This bit controls Power Control VNEGS/VPOSS programming. When this bit = 0b, Voltage Control Byte 0 is disabled. When this bit = 1b, Voltage Control Byte 0 is enabled.

REG[032Ch] Default = 000	General Con 0h	figuration Rec	gister				Read/Write
	n/a	Area Coordinate End Size Select	te Area Coordinate Rotation S ct bits 1-0				
15	14	13	12	11	10	9	8
n/	′a	Display FIFO Thres	hold Select bits 1-0		. n	'a	
7	6	5	4	3	2	1	0
bit 10	Are Thi the pos Wh area Wh	a Coordinate E s bit selects wh area update or ition (REG[034 en this bit = 0b a update. en this bit = 1b a update.	End Size Select nether REG[03 the horizontal/ 40h] ~ REG[03 o, REG[0344h] o, REG[0344h]	; 44h] ~ REG[0 /vertical size o 342h]). ~ REG[0346h ~ REG[0346h	346h] define th f the area upda n] define the X n] define the ho	ne X/Y end co tte relative to t /Y end coordin prizontal/vertic	ordinates of he X/Y start nates for the cal size for the
bits 9-8	Are The (RE	a Coordinate R se bits select th G[0340h] ~ R <i>Table 10-24</i> REG[0320	Rotation Select he rotation mod EG[0346h]). <i>4 : Area Coor</i> Ch] bits 9-8 00b	bits [1:0] de used to defi <i>rdinate Rotatic</i> Area Coordin	ne the area up on Selection ate Rotation	date input coor	rdinates
		1	0b	180	D°		
		1	1b	27	0°		

Display FIFO Almost Empty Threshold Select bits [1:0] These bits are used for debugging bits 5-4

These bits are used for debugging purposes only. These bits select the display FIFO condition that triggers a Display Pipe FIFO Underflow Interrupt which is indicated by REG[033Ah] bit 6.

Γ	REG[032Ch] bits 5-4	Display FIFO Threshold
Γ	00b (default)	Trigger REG[033Ah] bit 6 when FIFO is less than 1/2 full
Γ	01b	Trigger REG[033Ah] bit 6 when FIFO is less than 1/4 full
Ī	10b	Trigger REG[033Ah] bit 6 when FIFO is less than 3/4 full
	11b	Trigger REG[033Ah] bit 6 when FIFO is not full

REG[032Eh]	REG[032Eh] LUT Mask Register												
Default = 000	00h	-					Read/Write						
LUT 15 Mask	LUT 14 Mask	LUT 13 Mask	LUT 12 Mask	LUT 11 Mask	LUT 10 Mask	LUT 9 Mask	LUT 8 Mask						
15	14	13	12	11	10	9	8						
LUT 7 Mask	LUT 6 Mask	LUT 5 Mask	LUT 4 Mask	LUT 3 Mask	LUT 2 Mask	LUT 1 Mask	LUT 0 Mask						
7	6	5	4	3	2	1	0						

bits 15-0

LUT [15:0] Mask

These bits specify which LUTs (0-15) are included in the available status of the Masked LUT Status bit, REG[0338h] bit 6.

When this bit = 0b, the available status of LUTx is not included in REG[0338h] bit 6. When this bit = 1b, the available status of LUTx is included in REG[0338h] bit 6.

10.3.18 Display Engine: Control/Trigger Registers

REG[0330h] Default = 000	Update Buffe 0h	r Configuratio	on Register				Read/Write			
Display Engine Software Reset (WO)		n/a		Reserved						
15	14	13	12	11	10	9	8			
LUT Auto Select Enable	Reserved		n/a	LUT Index Format Select bits 2-0						
7	6	5	4	3	2	1	0			
bit 15	Disj This REC Wri Wri	play Engine So s bit performs a G[0350h] to the ting a 0b to thi ting a 1b to thi	oftware Reset (a software rese e default value s bit has no ef s bit initiates a	(Write Only) et of the displa e. fect. a software rese	y engine and r t of the display	esets the value y engine.	eof			
bit 11-8	Res The	erved default value	for these bits i	s 0000b.						
bit 7	LU' This Disj ava igno Wh Wh	LUT Auto Select Enable This bit determines whether the Look-Up Tables (LUTs) are manually selected using the Display Update LUT Select bit (REG[0334h] bits 7-4) or automatically selected from an available LUT. If Auto LUT Select is enabled, the Display Update LUT Select bits are ignored. When this bit = 0b, LUT auto select is disabled. When this bit = 1b, LUT auto select is enabled.								
bit 6	Res The	erved default value	for th <mark>is</mark> bit is 0	b.						
bits 2-0	LU' The	Index Forma se bits select th Table 1	t Select bits [2 ne index forma 0-26 : LUT L	:0] at for the Look ndex Format S	-Up Tables (L election	UTs).				
		REG[0330	0h] bits 2 <mark>-0</mark>	LUT Index	<pre>c Format</pre>					
		00)0b	P2	N					
		00)1b	P2	D					
		0,	10b	P3	N					
		0'	11b	P3	D					
		1()0b	P4	N					
		1()1b	P4	D					
		11	10b	P5	N					
		11	11b	Rese	rved					

Default = 000	Oh		and Rogiotoi				Read/Write
			n,	/a			
15	14	13	12	11	10	9	8
7	6	5			2	1	0
vits 7-0	Upd The REC	late Buffer Piz se bits specify G[0334h] bits	xel Set Value bi the pixel value 3-1 = 001b.	ts [7:0] e for the Upda	te Buffer Set V	alue Refresh o	operation,
REG[0334h] I Default = 000	Display Engir 0h	ne Control/Tr	igger Register				Write/Read
3-Wire Chip Power Control Enable	Border Update Enable	Update Rectan	gle Mode bits 1-0		Display Update Wav	eform Mode bits 3-0)
15	14	13	12	11	10	9	8
	Display Update L	UT Select bits 3-0		C	peration Mode bits 2	-0	Operation Trigge (WO)
7	6	5	4	3	2	1	0
nt 1 <i>3</i>	5-W This mat 3-W Who Who	s bit is only ac bit is only ac bit is bit con bit chip (using this bit = 0 bit this bit = 1	trols the 3-Wire b, the 3-Wire b, the 3-Wire b, the 3-Wire	Waveform dat e Chip power weform data) hip power cou hip power cou	a format is vers control sequence on every displa ntrol sequence i ntrol sequence i	ion 1 (voltage we used for pro- by update trigg is disabled. is enabled.	e control for- ogramming th ger.
sit 14	Bor This Who Who	der Update En s bit controls l en this bit $= 0$ en this bit $= 1$	hable border updates. b, the border is b, the border is	not updated o updated on th	n the next disp e next display	lay update (di update (enable	sabled). ed).
vits 13-12	Upd The Upd Upd rect	late Rectangle se bits are use late Buffer Se late, or Partial angle. Tabl	Mode bits [1:0 d when the sele t Value Refresh Display Updat e 10-27 : Upd)] ected operation , Update Buff ie. These bits is ate Rectangle	n mode (see RE er Image Buffe select the metho <i>Mode</i>	G[0334h] bits r Refresh, Ful od used to def	s 3-1) is set fo ll Display ïne the update
			1	9			

REG[0334n] bits 13-12		334nj bits 13-12	Update Rectangle Mode
		00b	Full Display Size Update
		01b	Host X/Y Start/End positions are used (see REG[0348h] ~ REG[034Eh]
		10b	X/Y Start/End positions are specified by REG[0340h] ~ REG[0346h]
		11b	Reserved

bits 11-8

Display Update Waveform Mode Select bits [3:0]

These bits are only used for Operation Modes 3 and 4 (REG[0334h] bits 3-1 = 011b and 100b). These bits select the Waveform Mode for the display update.

bits 7-4	Display Update LUT Select bits [3:0]
	These bits are only used for Operation Modes 3 and 4 (REG[0334h] bits 3-1 = 011b and
	100b). These bits select the LUT (from LUT0 to LUT15) that is used for the display
	update. If the LUT Auto Select Enable bit is set (REG[0330h] bit $7 = 1b$), these bits are
	ignored and the LUT is automatically selected.
bits 3-1	Operation Mode Select bits [2:0]
	These bits select the operation mode that is triggered when the Operation Write Trigger bit
	is set, $REG[0334h]$ bit $0 = 1b$.

REG[0334h] bits 3-1	Operation Mode					
000b	Waveform Header Read					
001b	Update Buffer Set Value Refresh					
010b	Update Buffer Image Buffer Refresh					
011b	Full Display Update					
100b	Partial Display Update					
101b	Gate Driver Clear Operation					
110b ~ 111b	Reserved					

Table 10-28 : Operation Mode Selection

bit 0

Operation Write Trigger (Write Only)

This bit triggers a new operation as selected by REG[0334h] bits 3-1. If a new operation is triggered while the Operation Trigger Busy bit is set (REG[0338h] bit 0 = 1b), the operation trigger is ignored and an Operation Trigger Error Interrupt occurs (see REG[033Ah] ~ REG[033Ch] bit 8).

Writing a 0b to this bit has no effect. Writing a 1b to this bit triggers a new operation.

10.3.19 Display Engine: Update Buffer Status Registers

REG[0336h] Lookup Table Status Register Default = 0000h Read Only							
LUT15 Frame Update Busy	LUT14 Frame Update Busy	LUT13 Frame Update Busy	LUT12 Frame Update Busy	LUT11 Frame Update Busy	LUT10 Frame Update Busy	LUT9 Frame Update Busy	LUT8 Frame Update Busy
15	14	13	12	11	10	9	8
LUT7 Frame Update Busy	LUT6 Frame Update Busy	LUT5 Frame Update Busy	LUT4 Frame Update Busy	LUT3 Frame Update Busy	LUT2 Frame Update Busy	LUT1 Frame Update Busy	LUT0 Frame Up <mark>da</mark> te Busy
7	6	5	4	3	2	1	0

bits 15-0

bit 10

LUT[15:0] Frame Update Busy (Read Only)

These bits indicate the status of the LUTx frame update. When a display update command for the corresponding LUT is issued, the LUT status will remain busy until all frames (N-Frames) have been transferred to the display.

When this bit = 0b, the corresponding LUT is not in use (idle).

When this bit = 1b, the corresponding LUT is in use (busy updating).

REG[0338h] Display Engine Busy Status Register							
Default = 0000h Re						Read/Write	
n/a		Serial Flash Checksum Error - N-Frame Compressed Data	Serial Flash Checksum Error - Region Pointer	Serial Flash Checksum Error - Mode Table	Serial Flash Checksum Error - Temperature Region	Serial Flash Checksum Error - Waveform Header	
15	14	13	12	11	10	9	8
n/a	Masked LUT Available Status (RO)	LUT Available Status <mark>(RO)</mark>	Border Frame Busy (RO)	Display Frame Busy <mark>(RO)</mark>	Update Buffer Refresh Status (RO)	1 Frame Memory Access Busy (RO)	Operation Trigger Busy (RO)
7 6 5		4	3	2	1	0	
bit 12	Seri	al Flash Checl	ksu <mark>m</mark> Error - N	I-Frame Comp	ressed Data		

 bit 12
 Serial Flash Checksum Error - Nerrane Compressed Data

 This bit indicates whether a Serial Flash Checksum Error has occurred in the N-Frame Compressed Data.

 When this bit = 0b, a serial flash checksum error has not occurred.

 When this bit = 1b, a serial flash checksum error has occurred.

 To clear this status bit, write a 1b to this bit.

 bit 11
 Serial Flash Checksum Error - Region Pointer

 This bit indicates whether a Serial Flash Checksum Error has occurred in the Region Pointer.

When this bit = 0b, a serial flash checksum error has not occurred. When this bit = 1b, a serial flash checksum error has occurred.

To clear this status bit, write a 1b to this bit.

Serial Flash Checksum Error - Mode Table This bit indicates whether a Serial Flash Checksum Error has occurred in the Mode Table. When this bit = 0b, a serial flash checksum error has not occurred. When this bit = 1b, a serial flash checksum error has occurred.

To clear this status bit, write a 1b to this bit.

bit 9	Serial Flash Checksum Error - Temperature Region This bit indicates whether a Serial Flash Checksum Error has occurred in the Temperature Region. When this bit = 0b, a serial flash checksum error has not occurred. When this bit = 1b, a serial flash checksum error has occurred.
	To clear this status bit, write a 1b to this bit.
bit 8	Serial Flash Checksum Error - Waveform Header This bit indicates whether a Serial Flash Checksum Error has occurred in the Waveform Header. When this bit = 0b, a serial flash checksum error has not occurred. When this bit = 1b, a serial flash checksum error has occurred.
	To clear this status bit, write a 1b to this bit.
bit 6	Masked LUT Available Status (Read Only) This bit indicates whether any of the LUTs (0-15) selected by the LUT Mask bits (REG[032Eh] bits 15-0) are currently available. When this bit = 0b, none of the selected LUTs are available. When this bit = 1b, at least one of the selected LUTs is available.
bit 5	LUT Available Status (Read Only) This bit indicates whether any LUTs are currently available. The number of available LUTs depends on the LUT Index Format, REG[0330h] bits 2-0. For P4D and P5N for- mats, only the first 4 LUTs are available. For all other formats, all 16 LUTs are available. When this bit = 0b, no LUTs are available. When this bit = 1b, at least one LUT is available.
bit 4	Border Frame Busy (Read Only) This bit indicates whether border frames are being output. When this bit = 0b, border frames are not being output (idle). When this bit = 1b, border frames are being output (busy).
bit 3	Display Frame Busy (Read Only) This bit indicates whether display frames are being output. When this bit = 0b, display frames are not being output (idle). When this bit = 1b, display frames are being output (busy).
bit 2	Update Buffer Refresh Status (Read Only) This bit indicates the status of update buffer refresh operations where the update buffer is written with new values. When this bit = 0b, the update buffer is not being refreshed. When this bit = 1b, the update buffer is being refreshed.
bit 1	 Frame Memory Access Busy (Read Only) This bit indicates whether the memory is being accessed and will be set during any update buffer related memory access, including memory reads for display output. When this bit = 0b, memory is not being accessed (idle). When this bit = 1b, memory is being accessed (busy).

bit 0

Operation Trigger Busy (Read Only)

This bit indicates the status of the current operation (see (REG[0334h] bits 3-1) which is triggered by the Operation Write Trigger, REG[0334h] bit 0. While the selected operation is completed, this bit is automatically reset to 0b. If a new operation is triggered while this bit is set to 1b, the operation trigger is ignored and an Operation Trigger Error Interrupt occurs (see REG[033Ah] ~ REG[033Ch] bit 8).

When this bit = 0b, an operation is not being processed (idle). When this bit = 1b, an operation is being processed (busy).

10.3.20 Display Engine: Interrupt Registers

REG[033Ah] Display Engine Interrupt Raw Status Register Default = 0000h Read/Write Image Buffer Serial Flash Entry Count Update Memory **Temperature Out** LUT Request Operation Trigger Mismatch n/a Incomplete Checksum Error of Range Interrupt Error Interrupt Error Interrupt Interrupt Raw Raw Status Interrupt Raw Interrupt Raw Raw Status Raw Status Status Status Status 15 14 13 12 10 9 8 11 One LUT **Display Pipe FIFO** All Frames **Display Output 1** Update Buffer LUT Busy Conflict N-Frame Display Operation Trigger Update Buffer Underflow Frame Complete Complete Refresh Done Changed Interrupt Detected Interrupt Complete Done Interrupt Interrupt Raw Interrupt Raw Interrupt Raw Interrupt Raw Raw Status Interrupt Raw Raw Status Raw Status Status Status Status Status Status 7 6 5 4 3 2 0 1 bit 13 Image Buffer Update Incomplete Interrupt Raw Status This bit indicates the raw status of the Image Buffer Update Incomplete Interrupt and is not masked by the Image Buffer Update Incomplete Interrupt Enable bit, REG[033Eh] bit 13. This interrupt occurs when the Display Engine begins reading data from the image buffer before the Host has completely written updated image data to the same buffer. When this bit = 0b, a Image Buffer Update Incomplete Interrupt has not occurred. When this bit = 1b, a Image Buffer Update Incomplete Interrupt has occurred. To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 13. bit 12 Serial Flash Memory Checksum Error Interrupt Raw Status This bit indicates the raw status of the Serial Flash Memory Checksum Error Interrupt and is not masked by the Serial Flash Memory Checksum Error Interrupt Enable bit, REG[033Eh] bit 12. To determine the cause of this interrupt, refer to the Serial Flash Memory Checksum Error Status bits, REG[0338h] bits 12-8. When this bit = 0b, a Serial Flash Memory Checksum Error Interrupt has not occurred. When this bit = 1b, a Serial Flash Memory Checksum Error Interrupt has occurred. To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 12. bit 11 Entry Count Mismatch Interrupt Raw Status This bit indicates the raw status of the Entry Count Mismatch Interrupt and is not masked by the Entry Count Mismatch Interrupt Enable bit, REG[033Eh] bit 11. This interrupt occurs when an unsupported entry count (see REG[0354h] bits 3-2) is selected for a Look-Up Table Index Format (see REG[0330h] bits 2-0). An entry count of 256 is only supported for index formats P2N, P2D, P3N, P3D, and P4N. An entry count of 1024 is only supported for index formats P4D and P5N. If a mismatch happens this bit is set and the update operation does not start. When this bit = 0b, an Entry Count Mismatch Interrupt has not occurred. When this bit = 1b, an Entry Count Mismatch Interrupt has occurred. To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 11.

bit 10	Temperature Out of Range Interrupt Raw Status This bit indicates the raw status of the Temperature Out of Range Interrupt and is not masked by the Temperature Out of Range Interrupt Enable bit, REG[033Eh] bit 10. This interrupt occurs during a display frame request when the temperature is greater than, or less than, the temperature regions from the Waveform Table. When this bit = 0b, a Temperature Out of Range Interrupt has not occurred. When this bit = 1b, a Temperature Out of Range Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 10.
bit 9	LUT Request Error Interrupt Raw Status This bit indicates the raw status of the LUT Request Error Interrupt and is not masked by the LUT Request Error Interrupt Enable bit, REG[033Eh] bit 9. This interrupt occurs an invalid LUT is requested by a triggered operation. An invalid LUT request happens when the requested LUT is currently in use (busy) or when auto LUT selection is enabled (REG[0330h] bit 7 = 1b) and no free LUTs are available. Note that for P5N and P4D index formats (see REG[0330h] bits 2-0), only the first four LUTs (0, 1, 2, and 3) are available. When this bit = 0b, a LUT Request Error Interrupt has not occurred. When this bit = 1b, a LUT Request Error Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 9.
bit 8	Operation Trigger Error Interrupt Raw Status This bit indicates the raw status of the Operation Trigger Error Interrupt and is not masked by the Operation Trigger Error Interrupt Enable bit, REG[033Eh] bit 8. This interrupt occurs when a new operation is triggered (REG[0334h] bit 0 = 1b) while another opera- tion is already being processed. If this happens, this bit is set and the operation trigger is ignored. When this bit = 0b, an Operation Trigger Error Interrupt has not occurred. When this bit = 1b, an Operation Trigger Error Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 8.
bit 7	LUT Busy Conflict Detected Interrupt Raw Status This bit indicates the raw status of the LUT Busy Conflict Detected Interrupt and is not masked by the LUT Busy Conflict Detected Interrupt Enable bit, REG[033Eh] bit 7. This interrupt occurs during image buffer updates when a pixel update is required and the same pixel is currently being used for frame display (using another LUT). When this bit = 0b, a LUT Busy Conflict Detected Interrupt has not occurred. When this bit = 1b, a LUT Busy Conflict Detected Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 7.

bit 6	Display Pipe FIFO Underflow Interrupt Raw Status This bit indicates the raw status of the Display Pipe FIFO Underflow Interrupt and is not masked by the Display Pipe FIFO Underflow Interrupt Enable bit, REG[033Eh] bit 6. This interrupt occurs when a new operation is triggered (REG[0334h] bit 0 = 1b) and a display pipe underflow error occurs. When this bit = 0b, a Display Pipe FIFO Underflow Interrupt has not occurred. When this bit = 1b, a Display Pipe FIFO Underflow Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 6.
bit 5	All Frames Completed Interrupt Raw Status This bit indicates the raw status of the All Frames Completed Interrupt and is not masked by the All Frames Completed Interrupt Enable bit, REG[033Eh] bit 5. This interrupt occurs at the end of a display output operation when all frames are completed. When this bit = 0b, an All Frames Completed Interrupt has not occurred. When this bit = 1b, an All Frames Completed Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 5.
bit 4	Update Buffer Changed Interrupt Raw Status This bit indicates the raw status of the Update Buffer Changed Interrupt and is not masked by the Update Buffer Changed Interrupt Enable bit, REG[033Eh] bit 4. This interrupt occurs on every write to the update buffer and may trigger multiple times even when the update buffer has not been completely updated. When this bit = 0b, an Update Buffer Changed Interrupt has not occurred. When this bit = 1b, an Update Buffer Changed Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 4.
bit 3	One LUT N-Frame Display Complete Interrupt Raw Status This bit indicates the raw status of the One LUT N-Frame Display Complete Interrupt and is not masked by the One LUT N-Frame Display Complete Interrupt Enable bit, REG[033Eh] bit 3. This interrupt occurs when the N-Frames required for a LUT to update a pixel or pixels completes. When this bit = 0b, a One LUT N-Frame Display Complete Interrupt has not occurred. When this bit = 1b, a One LUT N-Frame Display Complete Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 3.
bit 2	Display Output 1 Frame Complete Interrupt Raw Status This bit indicates the raw status of the Display Output 1 Frame Complete Interrupt and is not masked by the Display Output 1 Frame Complete Interrupt Enable bit, REG[033Eh] bit 2. This interrupt occurs when display output of 1 Frame to the output Gate and Source drivers completes. When this bit = 0b, a Display Output 1 Frame Complete Interrupt has not occurred. When this bit = 1b, a Display Output 1 Frame Complete Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 2.

bit 1	Update Buffer Refresh Done Interrupt Raw Status
	This bit indicates the raw status of the Update Buffer Refresh Done Interrupt and is not
	masked by the Update Buffer Refresh Done Interrupt Enable bit, REG[033Eh] bit 1. This
	interrupt occurs when an update buffer refresh operation (Set Value, Refresh, Partial
	Update, or Full Update; see REG[0334h] bits 3-1) completes.
	When this bit = 0b, an Update Buffer Refresh Done Interrupt has not occurred.
	When this bit = 1b, an Update Buffer Refresh Done Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[033Ch] bit 1.
bit 0	Operation Trigger Done Interrupt Raw Status
	This bit indicates the raw status of the Operation Trigger Done Interrupt and is not masked
	by the Operation Trigger Done Interrupt Enable bit, REG[033Eh] bit 0. This interrupt
	occurs when the operation triggered by REG[0334h] bit 0 is completes.
	When this bit = 0b, an Operation Trigger Done Interrupt has not occurred.
	When this bit = 1b, an Operation Trigger Done Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or **REG**[033Ch] bit 0.

				<u></u>			
REG[033Ch]	REG[033Ch] Display Engine Interrupt Masked Status Register						
Delault = 000	011			· · · ·			Reau/ White
n/a		Image Buffer Update Incomplete Interrupt Masked Status	Serial Flash Memory Checksum Error Interrupt Masked Status	Entry Count Mismatch Interrupt Masked Status	Temperature Out of Range Interrupt Masked Status	LUT Request Error Interrupt Masked Status	Operation Trigger Error Interrupt Masked Status
15	14	13	12	11	10	9	8
LUT Busy Conflict Detected Interrupt Masked Status	Display Pipe FIFO Underflow Interrupt Masked Status	All Frames Complete Interrupt Masked Status	Update Buffer Changed Interrupt Masked Status	One LUT N-Frame Display Complete Interrupt Masked Status	Display Output 1 Frame Complete Interrupt Masked Status	Update Buffer Refresh Done Interrupt Masked Status	Operation Trigger Done Interrupt Masked Status
7	6	5	4	3	2	1	0

bit 13

Image Buffer Update Incomplete Interrupt Masked Status

This bit indicates the masked status of the Image Buffer Update Incomplete Interrupt (see REG[033Eh] bit 13). This interrupt occurs when the Display Engine begins reading data from the image buffer before the Host has completely written updated image data to the same buffer.

When this bit = 0b, a Image Buffer Update Incomplete Interrupt has not occurred. When this bit = 1b, a Image Buffer Update Incomplete Interrupt has occurred.



To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 13.

Serial Flash Memory Checksum Error Interrupt Masked Status

This bit indicates the masked status of the Serial Flash Memory Checksum Error Interrupt (see REG[033Eh] bit 12). To determine the cause of this interrupt, refer to the Serial Flash Memory Checksum Error Status bits, REG[0338h] bits 12-8.

When this bit = 0b, a Serial Flash Memory Checksum Error Interrupt has not occurred. When this bit = 1b, a Serial Flash Memory Checksum Error Interrupt has occurred.

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 12.

bit 11	Entry Count Mismatch Interrupt Masked Status This bit indicates the masked status of the Entry Count Mismatch Interrupt (see REG[033Eh] bit 11). This interrupt occurs when an unsupported entry count (see REG[0354h] bits 3-2) is selected for a Look-Up Table Index Format (see REG[0330h] bits 2-0). An entry count of 256 is only supported for index formats P2N, P2D, P3N, P3D, and P4N. An entry count of 1024 is only supported for index formats P4D and P5N. If a mis- match happens this bit is set and the update operation does not start. When this bit = 0b, an Entry Count Mismatch Interrupt has not occurred. When this bit = 1b, an Entry Count Mismatch Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 11.
bit 10	Temperature Out of Range Interrupt Masked Status This bit indicates the masked status of the Temperature Out of Range Interrupt (see REG[033Eh] bit 10). This interrupt occurs during a display frame request when the tem- perature is greater than, or less than, the temperature regions from the Waveform Table. When this bit = 0b, a Temperature Out of Range Interrupt has not occurred. When this bit = 1b, a Temperature Out of Range Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 10.
bit 9	LUT Request Error Interrupt Masked Status This bit indicates the masked status of the LUT Request Error Interrupt (see REG[033Eh] bit 9). This interrupt occurs an invalid LUT is requested by a triggered operation. An invalid LUT request happens when the requested LUT is currently in use (busy) or when auto LUT selection is enabled (REG[0330h] bit 7 = 1b) and no free LUTs are available. Note that for P5N and P4D index formats (see REG[0330h] bits 2-0), only the first four LUTs (0, 1, 2, and 3) are available. When this bit = 0b, a LUT Request Error Interrupt has not occurred. When this bit = 1b, a LUT Request Error Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 9.
bit 8	Operation Trigger Error Interrupt Masked Status This bit indicates the masked status of the Operation Trigger Error Interrupt (see REG[033Eh] bit 8). This interrupt occurs when a new operation is triggered (REG[0334h] bit $0 = 1b$) while another operation is already being processed. If this happens, this bit is set and the operation trigger is ignored. When this bit = 0b, an Operation Trigger Error Interrupt has not occurred. When this bit = 1b, an Operation Trigger Error Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 8.

bit 7	LUT Busy Conflict Detected Interrupt Masked Status This bit indicates the masked status of the LUT Busy Conflict Detected Interrupt (see REG[033Eh] bit 7). This interrupt occurs during image buffer updates when a pixel update is required and the same pixel is currently being used for frame display (using another LUT). When this bit = 0b, a LUT Busy Conflict Detected Interrupt has not occurred. When this bit = 1b, a LUT Busy Conflict Detected Interrupt has occurred.
bit 6	To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 7. Display Pipe FIFO Underflow Interrupt Masked Status This bit indicates the masked status of the Display Pipe FIFO Underflow Interrupt (see REG[033Eh] bit6). This interrupt occurs when a new operation is triggered (REG[0334h] bit 0 = 1b) and a display pipe underflow error occurs. When this bit = 0b, a Display Pipe FIFO Underflow Interrupt has not occurred. When this bit = 1b, a Display Pipe FIFO Underflow Interrupt has occurred.
bit 5	To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 6. All Frames Completed Interrupt Masked Status
	 This bit indicates the masked status of the All Frames Completed Interrupt (see REG[033Eh] bit 5). This interrupt occurs at the end of a display output operation when all frames are completed. When this bit = 0b, an All Frames Completed Interrupt has not occurred. When this bit = 1b, an All Frames Completed Interrupt has occurred. To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 5.
bit 4	Update Buffer Changed Interrupt Masked Status This bit indicates the masked status of the Update Buffer Changed Interrupt (see REG[033Eh] bit 4). This interrupt occurs on every write to the update buffer and may trig- ger multiple times even when the update buffer has not been completely updated. When this bit = 0b, an Update Buffer Changed Interrupt has not occurred. When this bit = 1b, an Update Buffer Changed Interrupt has occurred.
bit 3	One LUT N-Frame Display Complete Interrupt Masked Status This bit indicates the masked status of the One LUT N-Frame Display Complete Interrupt (see REG[033Eh] bit 3). This interrupt occurs when the N-Frames required for a LUT to update a pixel or pixels completes. When this bit = 0b, a One LUT N-Frame Display Complete Interrupt has not occurred. When this bit = 1b, a One LUT N-Frame Display Complete Interrupt has occurred.
	To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 3.

bit 2	Display Output 1 Frame Complete Interrupt Masked Status This bit indicates the masked status of the Display Output 1 Frame Complete Interrup (see REG[033Eh] bit 2). This interrupt occurs when display output of 1 Frame to the put Gate and Source drivers completes. When this bit = 0b, a Display Output 1 Frame Complete Interrupt has not occurred. When this bit = 1b, a Display Output 1 Frame Complete Interrupt has occurred.				
	To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 2.				
bit 1	Update Buffer Refresh Done Interrupt Masked Status This bit indicates the masked status of the Update Buffer Refresh Done Interrupt (see REG[033Eh] bit 1). This interrupt occurs when an update buffer refresh operation (Set Value, Refresh, Partial Update, or Full Update; see REG[0334h] bits 3-1) completes. When this bit = 0b, an Update Buffer Refresh Done Interrupt has not occurred. When this bit = 1b, an Update Buffer Refresh Done Interrupt has occurred.				
	To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 1.				
bit 0	Operation Trigger Done Interrupt Masked Status This bit indicates the masked status of the Operation Trigger Done Interrupt (see REG[033Eh] bit 0). This interrupt occurs when the operation triggered by REG[0334h] bit 0 is completes. When this bit = 0b, an Operation Trigger Done Interrupt has not occurred. When this bit = 1b, an Operation Trigger Done Interrupt has occurred.				

To clear this status bit, write a 1b to either this bit or REG[033Ah] bit 0.

REG[033Eh] Display Engine Interrupt Enable Register Default = 0000h

Default = 0000h				Read Only			
n/a		Image Buffer Update Incomplete Interru <mark>pt Enable</mark>	Serial Flash Memory Checksum Error Interrupt Enable	Entry Count Mismatch Interrupt Enable	Temperature Out of Range Interrupt Enable	LUT Request Error Interrupt Enable	Operation Trigger Error Interrupt Enable
15	14	13	12	11	10	9	8
LUT Busy Conflict Detected Interrupt Enable	Display Pipe FIFO Underflow Interrupt Enable	All Frames Complete Interrupt Enable	Update Buffer Changed Interrupt Enable	One LUT N-Frame Display Complete Interrupt Enable	Display Output 1 Frame Complete Interrupt Enable	Update Buffer Refresh Done Interrupt Enable	Operation Trigger Done Interrupt Enable
7	6	5	4	3	2	1	0

bit 13

Image Buffer Update Incomplete Interrupt Enable

This bit controls whether the Image Buffer Update Incomplete Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 13 (unmasked) or REG[033Ch] bit 13 (masked). When this bit = 0b, the interrupt is disabled.

When this bit = 1b, the interrupt is enabled.
bit 12	Serial Flash Memory Checksum Error Interrupt Enable This bit controls whether the Serial Flash Memory Checksum Error Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 12 (unmasked) or REG[033Ch] bit 12 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 11	Entry Count Mismatch Interrupt Enable This bit controls whether the Entry Count Mismatch Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be deter- mined by reading REG[033Ah] bit 11 (unmasked) or REG[033Ch] bit 11 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 10	Temperature Out of Range Interrupt Enable This bit controls whether the Temperature Out of Range Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 10 (unmasked) or REG[033Ch] bit 10 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 9	LUT Request Error Interrupt Enable This bit controls whether the LUT Request Error Interrupt triggers a Display Engine Inter- rupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 9 (unmasked) or REG[033Ch] bit 9 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 8	Operation Trigger Error Interrupt Enable This bit controls whether the Operation Trigger Error Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be deter- mined by reading REG[033Ah] bit 8 (unmasked) or REG[033Ch] bit 8 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 7	LUT Busy Conflict Detected Interrupt Enable This bit controls whether the LUT Busy Conflict Detected Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 7 (unmasked) or REG[033Ch] bit 7 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 6	Display Pipe FIFO Underflow Interrupt Enable This bit controls whether the Display Pipe FIFO Underflow Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 6 (unmasked) or REG[033Ch] bit 6 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.

bit 5	All Frames Complete Interrupt Enable This bit controls whether the All Frames Complete Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be deter- mined by reading REG[033Ah] bit 5 (unmasked) or REG[033Ch] bit 5 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 4	Update Buffer Changed Interrupt Enable This bit controls whether the Update Buffer Changed Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be deter- mined by reading REG[033Ah] bit 4 (unmasked) or REG[033Ch] bit 4 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 3	One LUT N-Frame Display Complete Interrupt Enable This bit controls whether the One LUT N-Frame Display Complete Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 3 (unmasked) or REG[033Ch] bit 3 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 2	Display Output 1 Frame Complete Interrupt Enable This bit controls whether the Display Output 1 Frame Complete Interrupt triggers a Dis- play Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 2 (unmasked) or REG[033Ch] bit 2 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 1	Update Buffer Refresh Done Interrupt Enable This bit controls whether the Update Buffer Refresh Done Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be determined by reading REG[033Ah] bit 1 (unmasked) or REG[033Ch] bit 1 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.
bit 0	Operation Trigger Done Interrupt Enable This bit controls whether the Operation Trigger Done Interrupt triggers a Display Engine Interrupt (see REG[0240h] and REG[0242h]). The status of this interrupt can be deter- mined by reading REG[033Ah] bit 0 (unmasked) or REG[033Ch] bit 0 (masked). When this bit = 0b, the interrupt is disabled. When this bit = 1b, the interrupt is enabled.

10.3.21 Display Engine: Partial Update Configuration Register

Default = 0)000h	a opt		······						Read/Write
				Area U	pdate Pixel Rectang	ular X-Start Positic	n bits 11-8			
15		14		13	12	11	10		9	8
				Area U	Jpdate Pixel Rectang	ular X-Start Positi	on bits 7-0			
7		6		5	4	3	2		0	0
ts 15-0			Area U _I When th (REG[0 area to b	odate Pixe ne Update 334h] bits pe updated	l Rectangular Rectangle Mo 13-12 = 10b) l, relative to th	X-Start Posit de bits are se , these bits sp e top left of t	ion bits [15:0] t for user con ecify the X st he rotated ima	figured X art position age.	/Y Start	/End e rectangula
EG[0342 efault = 0	h] Are 0000h	a Upo	date Pixe	el Rectanç	gular Y-Start I	Register		2		Read/Write
15	1	14	1	Area U	pdate Pixel Rectang	ular Y-Start Positic	n bits 15-8	1	0	0
15		14		Area U	Jpdate Pixel Rectang	ular Y-Start Positi	on bits 7-0		9	0
7		6		5	4	3	2		0	0
FG[0344	h] Aro		area to l	be updated	l, relative to th	e top left of t	he rotated ima	art positio ige.		
efault = 0)000h			i Necianț	gular X-Ellu /		ize Register			Read/Write
	1		A	rea Update Pi	xel Rectangular X-E	nd Position / Horiz	ontal Size bits 15-8	i		
15		14		13 Aroa Undato P	12	I1 Ind Position / Horiz	10 Intel Size bits 7.0		9	8
7		6	<i>′</i>	5		3	2		0	0
s 15-0		C	Area U _I When tl (REG[0 zontal s top left	odate Pixe ne Update 334h] bits ize (see RI of the rota	l Rectangular Rectangle Mo 13-12 = 10b) EG[032Ch] bi ted image.	X-End Positi de bits are se these bits sp t 10) of the re	on / Horizonta t for user con ecify either th ectangular area	Il Size bit figured X le X end p a to be up	s [15:0] /Y Start position dated, r	/End or the hori- elative to th
EG[0346	h] Are	a Upo	date Pixe	el Rectang	gular Y-End /	Vertical Size	Register			
efault = (0000h									Read/Write
	1		I.	Area Update F	Pixel Rectangular Y-	End Position / Vert	ical Size bits 15-8	1	_ 1	-
15		14		13 Area Undate	12 Divel Postangular V	End Position / Vor	tical Size bits 7.0		9	8
7	ĺ	6	I	5	4	3	2		0	0
its 15-0	·		Area U _I When th	odate Pixe ne Update	l Rectangular Rectangle Mo	Y-End Position de bits are se	on / Vertical S t for user con	ize bits [1 figured X	5:0] /Y Start	/End

Default = 0)000h											R	ead On
					Host Pixe	el Rectangula	X-Start Position bit	s 15-8					
15		14		13		12	11		10		9		8
7	1	0	I.	-	Host Pix	el Rectangula	Ir X-Start Position bi	ts 7-0	0	1	0	1	0
1		0		5		4	3		Z		0		0
is 15-0			Host Pir When the bits 13- updated	xel Re he Upc 12 = 0 l.	ctangula late Rec 1b), the	ar X-Start etangle Mo se bits ind	Position bits ode bits are se licate the X sta	[15:0] t for co art pos	(Read opy Ho sition o	Only) ost X/Y of the re	Start/H ctangu	End (RI lar area	EG[0334 Ithat is
EG[034A efault = 0	h] Hos 0000h	t Pix	el Recta	ngula	r Y-Star	t Registe	r					R	ead On
					Host Pixe	el Rectangula	Y-Start Position bit	s 15-8					
15		14		13		12	11		10		9		8
					Host Pix	el Rectangula	r Y-Start Position bi	ts 7-0				1	
7		6		5		4	3		2		0		0
s 15-0			Host Pit When the bits 13- updated	xel Re he Upc 12 = 0 l.	ctangula late Rec 1b), the	ar Y-Start stangle Mo se bits ind	Position bits [ode bits are se licate the Y sta	15:0] t for co art pos	(Read opy Ho ition c	Only) ost X/Y of the re	Start/H ectangu	End (RI lar area	EG[033 a that is
EG[034C	Ch] Hos	t Pix	Host Piz When the bits 13- updated	xel Reche Upd $12 = 0$	ctangula late Rec 1b), the r X-End	ar Y-Start etangle Mo se bits ind Register	Position bits for the bits are selected bits are	15:0] t for co art pos	(Read opy Ho iition c	Only) ost X/Y of the re	Start/I	End (RI lar area	EG[033- a that is
EG[034C efault = 0	Ch] Hos 0000h	t Pix	Host Pir When the bits 13- updated	xel Reche Upd $12 = 0$ l.	ctangula date Rec 1b), the r X-End	ar Y-Start stangle Mo se bits ind Register	Position bits [ode bits are se licate the Y st	15:0] t for co art pos	(Read opy Ho ition c	Only) ost X/Y of the re	Start/Hectangu	End (RI lar area	EG[033 a that is
EG[034C efault = 0	ch] Hos 0000h		Host Pi When the bits 13- updated	xel Reche Upd $12 = 0$ l.	ctangula late Rec 1b), the r X-End Host Pix	ar Y-Start stangle Mo se bits ind Register el Rectangula	Position bits [ode bits are se licate the Y sta r X-End Position bits	15:0] t for co art pos s 15-8	(Read opy He ition c	Only) ost X/Y of the re	Start/I ectangu	End (RI lar area	EG[033 a that is
s 15-0 EG[034C efault = 0 15	Ch] Hos 0000h	it Pix	Host Pi When the bits 13- updated	xel Req he Upc 12 = 0 l. ngula	ctangula late Rec 1b), thes r X-End Host Pix Host Pix	ar Y-Start stangle Mo se bits ind Register el Rectangula 12 rel Rectangula	Position bits for the bits are selected bits are	15:0] t for co art pos s 15-8 	(Read opy Ho ition c	Only) ost X/Y of the re	Start/I ectangu	End (RI lar area	EG[033 a that is lead On
EG[034C efault = 0 15 7	ch] Hos 0000h 	t Pix 14 6	Host Pir When the bits 13- updated el Recta	xel Red he Upc 12 = 0 I. ngula 13 5	ctangula late Rec 1b), the: r X-End Host Pix Host Pix	ar Y-Start stangle Mo se bits ind Register el Rectangula 12 kel Rectangula 4	Position bits [ode bits are se licate the Y stand r X-End Position bits 11 ar X-End Position bits 3	15:0] t for co art pos s 15-8 l 	(Read opy Ho ition c 10	Only) 5st X/Y of the re	Start/I ectangu 9 0	End (RI lar area R	EG[033- a that is lead On 8 0
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Host Pixel Rectangular Y-End Position bits [15:0] (Read Only) When the Update Rectangle Mode bits are set for copy Host X/Y Start/End (REG[0334h] bits 13-12 = 01b), these bits indicate the Y end position of the rectangular area that is updated.

10.3.22 Display Engine: Serial Flash Waveform Registers

Dofoult = 00	N] Waveform H	eader Serial F	lash Address	Register 0			Pood/M/rito			
	0001						Reau/ White			
		Wa	aveform Header Serial	Flash Address bits 1	15-8					
15	14	13	12	11	10	9	8			
		W	aveform Header Seria	I Flash Address bits	7-0					
7	6	5	4	3	2	1	0			
REG[0352h Default = 00	1] Waveform H 000h	eader Serial F	lash Address	Register 0		•	Read/Write			
	n/a									
			n/	а						
15	14	13	n/ 12	a 11	10	9	8			
15	14	<mark> 13</mark> Wa	n/ 12 veform Header Serial	a 11 Flash Address bits 2	<u>10</u> 3-16	9	8			

REG[0352h] bits 7-0

REG[0350h] bits 15-0 Waveform Header Serial Flash Address bits [23:0] These bits store the Waveform Header start address in the Flash Memory.

REG[0354h] through REG[035Eh] are Reserved

These registers are Reserved and should not be written.

Chapter 11 Display Configurations

11.1 Display Memory Area Setup

The S1D13521 controller supports a single display region with destructive partial region writes only. A predefined memory start region can be defined using the Host commands (see Section 9.4, "Command List" on page 51). The memory start region is referenced as the Image Buffer Start Address position in the memory.



For any partial write using the predefined area (XStart, YStart, Width, and Height parameters), the S1D13521 automatically calculates the start memory address position.



Figure 11-2: Host Memory Area Setup

11.2 Display Memory Bpp Mode

This S1D13521 stores every pixel in unpacked 1 byte format. The following figure shows how data is formatted using this single byte storage.



Note

For 8 bpp mode, the LUT index format (REG[0330h] bits 2-0) determines which MSB bits are used.

- 5 bpp (G7-G3) 4 bpp – (G7-G4)
- 3 bpp (G7-G5)
- 2 bpp (G7-G6)

11.3 Host Interface Pixel Data Transfer Format

Data transfer from the Host interface always uses packed pixel format. Packed pixels are always arranged using the little endian arrangement. The following figure shows the host transfer data format of four pixel mode.



Figure 11-4: Host Interface Pixel Data Transfer Format

The packed pixel format requires certain limitations to be observed for all host image data transfers. The following size limitations must be observed for each bpp mode.

Table 11-1: Host Interface Pixel Data Transfer Limitations

Bpp Mode	Width limitation	Height limitation
2 bpp	Must be multiple of 8 pixels	Minimum of 1 Line
3 bpp	Must be multiple of 4 pixels	Minimum of 1 Line
4 bpp	Must be multiple of 4 pixels	Minimum of 1 Line
5/8 b <mark>p</mark> p	Must be multiple of 2 pixels	Minimum of 1 Line

11.4 Rotation Support

11.4.1 Rotation Introduction

Display panels are typically oriented in Landscape mode, where the Horizontal Size is larger than the Vertical Size. In this case, the display refresh occurs from Left to right and top to bottom.



Figure 11-5: Landscape (0 Degrees) Display

The S1D13521 supports rotation modes that allow 90°, 180°, and 270° rotation in a counter-clockwise direction. The rotation is done in hardware and is transparent to the user for all display buffer writes.

The actual address translation is performed during the Host Write and the image data is stored in memory in the rotated orientation.



Note

Memory Readback data does not support reverse-rotation.

11.4.2 90° Rotation

The following figure shows how the programmer sees a 600x800 portrait image and how the image is being displayed. The application image is written to the S1D13521 in the following sense: A–B–C–D. The display is refreshed in the following sense: B-D-A-C.



Figure 11-7: Relationship Between the Screen Image and the Image Refreshed in 90° Rotation

Programming



11.4.3 180° Rotation

The following figure shows how the programmer sees a 800x600 landscape image and how the image is being displayed. The application image is written to the S1D13521 in the following sense: A–B–C–D. The display is refreshed in the following sense: D-C-B-A.



Figure 11-8: Relationship Between the Screen Image and the Image Refreshed in 180° Rotation

Programming



11.4.4 270° Rotation

The following figure shows how the programmer sees a 600x800 portrait image and how the image is being displayed. The application image is written to the S1D13521 in the following sense: A–B–C–D. The display is refreshed in the following sense: C-A-D-B.



Figure 11-9: Relationship Between the Screen Image and the Image Refreshed in 270° Rotation

Programming

11.5 Window Area Position / Rotation

For a Windowed Area write operation when rotation is enabled, the X-Start, Y-Start, Width and Height settings must be specified relative to **the user's own reference point**.

11.5.1 90° Rotation

The following figure shows how the Windowed Area is rotated on the displayed image. The application Window Area is written to the S1D13521 in the following sense: a–b–c–d.



Figure 11-10: Relationship Between the Screen Window Area and the Image Refreshed in 90° Rotation

Programming

There are no special programming requirements other than enabling the rotation (see REG[0140h] bits 9-8). The start address and line offset are automatically calculated by the hardware.

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11.5.2 180° Rotation

The following figure shows how the Windowed Area is rotated on the displayed image. The application Window Area is written to the S1D13521 in the following sense: a-b-c-d.



Figure 11-11: Relationship Between the Screen Window Area and the Image Refreshed in 180° Rotation

Programming

11.5.3 270° Rotation

The following figure shows how the Windowed Area is rotated on the displayed image. The application Window Area is written to the S1D13521 in the following sense: a–b–c–d.



Figure 11-12: Relationship Between the Screen Window Area and the Image Refreshed in 270° Rotation

Programming

Chapter 12 Display Engine

TBD

Chapter 13 SPI Interface

13.1 Register Descriptions

13.1.1 SPI Flash Chip Select Control Register

The SPI Flash Chip Select Enable bit (REG[0208h] bit 0) is used to assert/deassert the SPICS_L pin. The value programmed to this bit is the inverse of the SPICS_L output. The default value of this bit is 0b (SPICS_L = 1) which disables chip select.

13.1.2 SPI Flash Control Register

The SPI Flash Control Register (REG[0204h]) configures the operation of the SPI Flash Memory interface. It has the following control bits:

- Bit 0 is the SPI Flash Enable bit and is set to 1b to enable the SPI Interface.
- Bits 2-1 are the SPI Flash Clock Phase Select and SPI Flash Clock Polarity Select bits which select the SPICLK phase and polarity. For a summary of the phase and polarity settings, see Table 10-19 "SPI Flash Clock Phase and Polarity," on page 100.
- Bits 5-3 are the SPI Flash Clock Divide Select bits for programming the SPICLK frequency.
- Bit 6 is the SPI Flash Read Command Select bit and is applicable only when bit 7 is 1b. It selects whether to use Normal Read or Fast Read commands when reading the Serial Flash Memory from the VBUS.
- Bit 7 is the SPI Flash Read Mode bit. When it is 0b, access to the external Serial Flash Memory is through firmware programming of the SPI registers. In this mode, control of the SPI interface engine is given to the SPI interface registers. When it is 1b, the Display Engine has control over the operation of Serial Flash Memory.

13.1.3 SPI Flash Write Data Register

This write only register (REG[0202h]) is used to trigger a byte serial transfer on the SPICLK/SPIO pins. Writing a byte value (with REG[0202h] bit 8 = 1b) to this register causes the byte value to be serial shifted out on SPICLK/SPIO.

13.1.4 SPI Flash Read Data Register

This read only register (REG[0200h]) is used to read byte data received from the SPI interface. In order to read a byte of data into this register, a "dummy" write to REG[0202h] must be performed (with REG[0202h] bit 8 = 0b).

13.1.5 SPI Flash Status Register

This read only register (REG[0206h]) provides status bits indicating the state of the SPI interface engine. The following status bits are available:

- Bit 0 is the SPI Flash Read Data Ready Flag. It is set to 1b whenever a new byte of data has been loaded into the SPI Flash Read Data register, REG[0200h]. This bit is cleared when REG[0200h] is read.
- Bit 1 is the SPI Flash Read Data Overrun Flag. It is set to 1b whenever a new byte of data is loaded into the SPI Flash Read Data register, REG[0200h], and the SPI Flash Read Data Ready Flag (bit 0) is still 1b (indicating that the previous byte has not yet been read out). This bit is cleared by reading REG[0200h].
- Bit 2 is the SPI Flash Write Data Register Empty Flag. It is set to 1b whenever the SPI Flash Write Data Register, REG[0202h], is empty. Writing a byte value to REG[0202h] will initially cause this bit to return 0b. When the byte value is transferred to the serial shift register, this bit is set to 1b again.
- Bit 3 is the SPI Flash Busy Flag. It is set to 1b when the SPI interface engine is busy shifting a byte of data in/out on the SPI interface.



13.2 Flash Memory Accesses using SPI Interface Registers

The following figures show the recommended sequences for accessing the Serial Flash Memory using the SPI interface registers. Before performing instruction sequences, the SPI interface must be configured using the SPI Flash Control Register, REG[0204h]. A Write Enable instruction sequence must have been executed before any Page Program instruction sequence.



Figure 13-1: Page Program (Write Data) Instruction Sequence



Chapter 14 Firmware Programming Guide

TBD

Chapter 15 Analog Power Supply Considerations

The PLL circuit is an analog circuit which is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of this circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for this circuit be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible.

The following are guidelines which, if followed, will result in cleaner power to the PLL circuit. This will result in a cleaner and more stable clock. Even a partial implementation of these guidelines will give results.



15.1 Guidelines for Analog Power Layout

Figure 15-1: Analog Power Layout

- Place the ferrite beads (L1 and L2) parallel to each other with minimal clearance between them. Both bypass caps (C2 and C3) should be as close as possible to the inductors. The traces from C3 to the power planes should be short parallel traces on the same side of the board with just the normal small clearance between them. Any significant loop area here will induce noise. If there is a voltage regulator on the board, try to run these power traces directly to the regulator instead of dropping to the power planes (still follow above rules about parallel traces).
- The analog ground point where bypass cap (C2) connects to the ground isolation inductor (L2) becomes the analog ground central point for a ground star topology. None of the components connect directly to the analog ground pin of the S1D13521 (PLLV_{SS}) except for a single short trace from C2 to the PLLV_{SS} pin. The ground side of the large bypass capacitor (C1) should also have a direct connection to the star point.

- The same star topology rules used for analog ground apply to the analog power connection where L2 connects to C2.
- All of the trace lengths should be as short as possible.
- If possible, have all the PLL traces on the same outside layer of the board. The only exception is C1, which can be put on the other side of the board if necessary. C1 does not have to be as close to the analog ground and power star points as the other components.
- If possible, include a partial plane under the PLL area only (area under PLL components and traces). The solid analog plane should be grounded to the C2 (bypass) pad. This plane won't help if it is too large. It is strictly an electrostatic shield against coupling from other layers' signals in the same board area. If such an analog plane is not possible, try to have the layer below the PLL components be a digital power plane instead of a signal layer.
- If possible, keep other board signals from running right next to PLL pin vias on any layer.
- Wherever possible use thick traces, especially with the analog ground and power star connections to either side of C2. Try to make them as wide as the component pads thin traces are more inductive.

It is likely that manufacturing rules will prohibit routing the ground and power star connections as suggested. For instance, four wide traces converging on a single pad could have reflow problems during assembly because of the thermal effect of all the copper traces around the capacitor pad. One solution might be to have only a single trace connecting to the pad and then have all the other traces connecting to this wide trace a minimum distance away from the pad. Another solution might be to have the traces connect to the pad, but with thermal relief around the pad to break up the copper connection. Ultimately the board must also be manufacturable, so best effort is acceptable.

S1D13521 Hardware Functional Specification (Rev. 0.05)



Chapter 16 Mechanical Data

Figure 16-1: PFBGA8UX 181-pin Package

16.1 Thermal Details

The thermal details for the PFBGA8UX 181-pin package are as follows:

 $\theta ja: 31^{\circ}C / W (max \pm 10^{\circ}C / W)$

Chapter 17 References

The following documents contain additional information related to the S1D13521. Document numbers are listed in parenthesis after the document name. All documents can be found at the Epson Research and Development Website at **www.erd.epson.com**.

• S1D13521 Product Brief (X88A-C-001-xx)

Change Record

X88A-A-001-00 Revision 0.05 - Issued: November 7, 2007

- All changes from the previous revision are Red
- section 2.1, changed source/gate driver interface descriptions to include "compatible devices"
- section 2.2, updated 16-bit Host Interface features list with comment about Command Mode and User programmed commands
- section 2.2, removed reference to register mode
- section 2.4, changed Power Management IC description to include "compatible devices"
- section 2.6, added reference to the LM75 in the I2C Thermal Sensor Temperature Reading Features section
- section 2.7, added the Auto Command Sequence Features section
- section 2.9, added Crystal Interface to the Clock Source Features section
- section 2.10, for the Miscellaneous Features section combined the power mode features into "Sleep and Standby Power Save Modes"
- section 3, added basic block diagram
- section 3.1, added typical system implementation
- section 4.2, added ILTR Cell Description
- section 4.2, updated the RESET# state of all pins-
- section 4.2, minor edits to clarify the pin descriptions
- section 4.2.7, separated the pin descriptions for SDCE_L[10:9] and SDCE_L[8:0] and added reference on the configurability of the pins
- section 4.2.10, added the OSCI and OSCO pins and pin descriptions to the Miscellaneous section
- section 4.2.10, added the CNF3 pin and pin description to the Miscellaneous section
- section 4.2.11, changed the SDRIOVDD power from "1.65-3.6V" to "1.8/3.3V", changed the PPIOVDD power from "3.3V" to "1.65-3.6V", changed the PIOVDD power from "3.3V" to "1.65-3.6V"
- section 4.2.11, added the OSCVDD and OSCVSS pins and pin descriptions to the Power and Ground section
- section 4,2,11, updated the number of balls for each power supply
- section 4.3, added new section summarizing the Configuration Pins
- section 4.4.2 ~ 4.4.3, reworded the table headings for the Source Driver Interface Bitwidth Select and Border Pin Interface Bitwidth Select tables
- section 5,1, added Absolute Maximum Ratings for OSC supply voltage
- section 5.2, added Recommended Operating Conditions for OSC supply voltage
- section 5.2, for the SDRIOVDD Recommended Operating Conditions changed the Min from "3.00" to "2.70"

- section 6.1.1, added OSC option to CLKI Input Requirements
- section 6.1.1, for the Clock Input Requirements table changed the t3 and t4 parameter max values from 5.0ns to 500ps
- section 6.1.1, for the Clock Input Requirements table changed the t5 and t6 parameter min/max values from -300/300ps to -150/150ps
- section 6.1.1, added note 6 about achieving the maximum possible PLL output frequency
- section 6.1.2, reserved the tPJref and tPDuty parameters from he PLL Clock Requirements table
- section 6.2, for the power-on/power-off sequence figures, clarified the maximum voltage allowed
- section 6.4.1, for the 16-bit Host timing updated the min timings for twl, twh, tw2r, tr2w, tr1, and trh
- section 6.4.1, for the 16-bit Host timing updated the min timing for tdht from "5ns" to "7ns"
- section 6.5, added Display Timing Register summary and added note
- section 6.5, for the Display Timing, the Line Sync Length formula changed to "((REG[0308h]) bits 7-0) x 4) + 2)"
- section 6.5.1, added example Frame Rate Calculation
- section 6.5.2, updated the Source Driver Display Timings
- section 6.5.3, updated the Gate Driver Display Timings
- section 6.6.1, for the PWR[3:0] Transition Sequence figure changed "Frame Clk" to "Line Clk"
- section 6.6.1, for the PWR[3:0] Transition Sequence clarified the text, added values for tu parameter, and removed td parameter
- section 6.6.2, for the PWRCOM Transition Sequence clarified the text, moved t1 in the figure, and added min values to the table
- section 7.1, added OSCI/OSCO to the Clock Tree Diagram
- section 8.1, clarified the S1D13521 power state descriptions
- section 9.1, updated the Host Cycle Sequences section
- section 9.4 ~ 9.5, updated the Command List section
- section 10, unreserved all registers from REG[0000h] ~ REG[0352h]
- REG[000Ah], changed System Status Register from "Read Only" to "Read/Write"
- REG[000Ah] bits 12-10, added the Power Save Status bits and bit description
- REG[000Ah] bit 0, added information to not access the synchronous registers or memory before the PLL output is stable
- REG[0014h] bits 14-8, revised the PLL Setting Example
- REG[0016h], changed default register value from "0000h" to "0002h"
- REG[0108h] bit 3, reserved this bit
- REG[0140h] bit 7, added the Packed Pixel Destination Start Address Select bit and bit description
- REG[0206h], changed default register value from "0000h" to "0004h"

- REG[0220h] ~ REG[0226h], changed the register description to refer to "3-Wire Chip Interface"
- REG[0240h] ~ REG[0244h], changed the register description to refer to "3-Wire Chip Interface"
- REG[0240h], REG[0242h], REG[0244h] bit 8, added the Host Memory Read/Write FIFO Error Interrupt raw status, masked status, and enable bits and bit descriptions
- REG[030Ch] bits 7-0, extended the Source Driver Output Size Select bits from "bits 6-0" to "bits 7-0"
- REG[030Eh] bits 15-11, added the Source Driver SDOED Delay bits and bit descriptions
- REG[030Eh] bit 10, added the Source Driver Double Data Rate Enable bit and bit description
- REG[030Eh] bits 7-4, added the Source Driver SDOEX Delay bits and bit descriptions
- REG[032Ah] bit 8, added the Voltage Control Byte Force Frame Wait bit and bit description
- REG[032Ah] bits 7-4, added the Voltage Control Byte Wait Select bits and bit description
- REG[032Eh], added the LUT Mask register
- REG[0330h] bit 15, for the Display Engine Software Reset bit description added register default value reset comment
- REG[0330h] bits 11-8, added these bits as Reserved bits
- REG[0334h] bit 15, changed the register description to refer to "3-Wire Chip Interface"
- REG[0338h] bit 6, added the Masked LUT Available Status bit and bit description
- REG[033Ah], REG[033Ch], REG[033Eh] bit 13, added the Image Buffer Update Incomplete Interrupt raw status, masked status, and enable bits and bit descriptions
- section 11, minor wording clarifications to the Display Configurations section
- section 11.1, adjusted the Image Area so it is not at the beginning of SDRAM
- section 13, minor wording clarifications to the SPI Interface section
- section 13.1, changed references from "SPICS#" to "SPICS_L"

X88A-A-001-00 Revision 0.04 - Issued: October 19, 2007

- All changes from the previous revision are Red
- section 4.2, updated cell descriptions table and cell descriptions for all pins
- section 4.2.1, updated RESET_L pin description to add cross reference to RESET_L Timing section
- section 4.2.2, removed the reference to CNF0
- section 4.2.2, changed HRDY pin type from "O" to "IO"
- section 4.2.2, clarified some of the Host Interface pin descriptions
- section 4.2.5, for the TI2CC and TI2CD pin descriptions added that they must be connected to PPIOVDD when they are not used
- section 4.2.8, changed PWR0, PWR1, PWR3 pin types from "O" to "IO"
- section 4.2.10, changed CNF1 pin description to be "Reserved. This pin must be connected to HIOVDD."

- section 4.2.10, for the CNF2 pin description added information that this pin must be connected to VSS
- section 4.2.11, for the PFBGA Pin# column clarified that the number only specifies the number of balls
- section 4.2.11, updated the "power" column for the COREVDD and PLLVDD pins from "1.5V" to "1.8V"
- section 4.3.1, reserved the host pin mapping section
- section 5, replaced DC Characteristics section
- section 5.3, added Electrical Characteristics tables for COREVDD and PLLVDD with TBD values
- section 6.1.1, for the Clock Input Requirements table changed foscmin from "1MHz" to "20MHz" and foscmax from "TBD" to "66.5MHz"
- section 6.1.2, for the PLL Clock section changed the PLL output clock frequency min from "TBD" to "40MHz"
- section 6.1.2, for the PLL Clock section changed the PLL duty cycle from "40/60" to "TBD" and changed the PLL output stable time from "TBD" to "200us"
- section 6.2, added Power-on/off Sequence timing section
- section 6.4, corrected the Host Timing diagram and table to use the correct host pin names
- section 7.1, replaced the Clock Tree Diagram
- section 7.1, reserved clock tree notes
- section 7.2, reserved the PLL Block Diagram
- section 8.1, changed "Init PLL" wait time to "200us"
- section 9 and 10, swapped Host Interface and Registers sections
- section 9, replaced the Host Interface section
- section 10, reserved references to Register Mode
- section 10, added REG[0000h] ~ REG[001Ah] and REG[0200h] ~ REG[020Fh] and updated the register descriptions accordingly
- REG[0010h] bits 5-0, changed PLL input clock range to "20 ~ 66.5MHz"
- REG[0018h] bit 4, added the Pixel Clock Divide Disable bit and bit description
- section 11.2, in the Display Memory Bpp Mode section updated the note that describes 8 bpp mode
- section 11, minor wording clarifications in the Display Configurations section
- section 12, added stub for Display Engine section
- section 13, added SPI Interface section
- section 15, added Analog Power Supply Considerations section
- section 16.1, added Thermal Details for the package
- removed Sales and Technical Support section and added Epson International Sales Operations back page

X88A-A-001-00 Revision 0.03 - Issued: September 10, 2007

- All changes from the previous revision are Red
- section 4.2.4, changed the SPIDCS_L and SPICLK pins from inputs to outputs
- section 4.2.8, updated Dialog DA8590 3-wire signal name and description for the PWR[0] and PWR[3] pins
- section 4.2.10, added the CLKI pin and description
- section 6.4, moved the display timings into the AC Timings section
- section 7.1, updated the clock tree diagram with 3-Wire Serial, Pixel, and I2C Thermal Sensor clock divide register changes
- section 10, various updates and clarifications to the Host Interface section
- section 14, added References section
- section 15, added Sales and Technical Support section

X88A-A-001-00 Revision 0.02 - Issued: July 23, 2007

- All changes from the previous revision are Red
- globally replace "Broadsheet" with "S1D13521"

X88A-A-001-00 Revision 0.01 - Issued: July 19, 2007

• initial draft of the S1D13521 specification

EPSON

International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.

HEADQUARTERS 2580 Orchard Parkway San Jose , CA 95131,USA Phone: +1-800-228-3964

FAX: +1-408-922-0238

SALES OFFICES Northeast

 301 Edgewater Place, Suite 210

 Wakefield, MA 01880, U.S.A.

 Phone: +1-800-922-7667
 FAX: +1-781-246-5443

EUROPE

EPSON EUROPE ELECTRONICS GmbH HEADQUARTERS Riesstrasse 15 80992 Munich, GERMANY Phone: +49-89-14005-0 FAX: +49-89-14005-110

ASIA

EPSON (CHINA) CO., LTD. 23F, Beijing Silver Tower 2# North RD DongSanHuan ChaoYang District, Beijing, CHINA Phone: +86-10-6410-6655 FAX: +86-10-6410-7320

SHANGHAI BRANCH

7F, High-Tech Bldg., 900, Yishan Road, Shanghai 200233, CHINA Phone: +86-21-5423-5522 FAX: +86-21-5423-5512

EPSON HONG KONG LTD.

20/F., Harbour Centre, 25 Harbour Road Wanchai, Hong Kong Phone: +852-2585-4600 FAX: +852-2827-4346 Telex: 65542 EPSCO HX

EPSON Electronic Technology Development (Shenzhen) LTD.

12/F, Dawning Mansion, Keji South 12th Road, Hi- Tech Park, Shenzhen Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

EPSON TAIWAN TECHNOLOGY & TRADING LTD.

14F, No. 7, Song Ren Road, Taipei 110 Phone: +886-2-8786-6688 FAX: +886-2-8786-6660

EPSON SINGAPORE PTE., LTD.

1 HarbourFront Place, #03-02 HarbourFront Tower One, Singapore 098633 Phone: +65-6586-5500 FAX: +65-6271-3182

SEIKO EPSON CORPORATION

KOREA OFFICE 50F, KLI 63 Bldg., 60 Yoido-dong Youngdeungpo-Ku, Seoul, 150-763, KOREA Phone: +82-2-784-6027 FAX: +82-2-767-3677

GUMI OFFICE

2F, Grand B/D, 457-4 Songjeong-dong, Gumi-City, KOREA Phone: +82-54-454-6027 FAX: +82-54-454-6093

SEIKO EPSON CORPORATION SEMICONDUCTOR OPERATIONS DIVISION

IC Sales Dept.

IC International Sales Group 421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN Phone: +81-42-587-5814 FAX: +81-42-587-5117