Low-temperature deposition of high-quality silicon dioxide by plasma-enhanced chemical vapor deposition

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Thin films of high-quality silicon dioxide have been deposited at low temperatures by plasma-enhanced chemical vapor deposition. A deposition rate much lower than that used in conventional plasma-enhanced processes is found to be crucial in obtaining material with reproducible, good properties. Controlled, slow deposition is achieved by using very low flow rates of reactive gases, together with a much higher flow of inert carrier gas to ensure uniformity. Films deposited at usual high deposition rates ($\sim$500 Å/min) exhibit irreproducible and poor electrical properties and are porous. Those deposited slowly ($\sim$60 Å/min) have very reproducible properties, are relatively dense and exhibit very good electrical integrity. Oxides deposited using a substrate temperature of 350 °C compare favorably with those deposited at 700°C using atmospheric-pressure chemical vapor deposition and can be deposited routinely over a wide range of oxide thickness. Deposition at 275 °C results in similar properties but with increased electron capture associated with deep bulk traps. Thicker layers can be deposited onto polycrystalline metal (sputtered films on glass substrates) without any deterioration in film properties. The as-deposited Si:SiO_2 interface state density is quite high ($\sim 10^{12}$ eV^{-1} cm^{-2}), although it is reduced to very respectable levels (in the mid 10^{10}–10^{11} eV^{-1} cm^{-2} range) by conventional postmetallization anneals. The suitability of these low-temperature oxides for thin film transistor applications is discussed.

I. INTRODUCTION

The deposition of insulators at low temperatures has applications in a number of semiconductor device technologies. For example, as secondary passivation layers, interlayer isolation, and lithographic masks in integrated circuits and also as primary gate dielectrics for thin film transistor (TFT) applications. One of the most widespread low-temperature deposition techniques is plasma-enhanced chemical vapor deposition (PECVD), where an rf discharge supplies the additional energy required to promote the chemical reaction. The properties of PECVD insulators have been extensively studied in recent years, particularly with regard to applications in the area of integrated circuits. These applications require control primarily of physical, mechanical, and chemical properties such as pinhole density, stress, and etch resistance, and most research to date has focused on silicon-based nitrides which are generally superior to oxides in these respects. There are numerous reports of these properties in the literature (see, for example, Refs. 1 and 2).

More recently, attention has turned to the use of plasma-deposited insulators as *primary* dielectrics in thin-film transistors based on amorphous or polycrystalline silicon. In the amorphous silicon case, both the semiconductor and the insulator are deposited at low temperatures by PECVD, which has enabled large arrays of TFTs to be fabricated on inexpensive glass substrates. By using the TFT array together with liquid crystal technology it is hoped that large-area flat panel displays can be fabricated at relatively low cost as an alternative to the cathode ray tube. A number of prototypes have already been developed.[3,4] The technology for depositing electronic grade hydrogenated amorphous silicon (*a*-Si:H) over large areas was developed for solar cell applications and is well advanced. However, the deposition of gate insulators with good electrical properties is not so well established, despite a large effort in the area of silicon nitride. This material, although used routinely and successfully for secondary insulation purposes, is far from ideal for use as a gate insulator. Electronic conduction, even in high-quality (high temperature CVD) Si_3N_4, is complex: Both electron and hole injection are important and a high density of bulk traps modulates the conductivity. This leads to an inherent problem in the control of threshold voltage and stability.

In contrast, electronic quality SiO_2 has much more desirable properties: Conduction is essentially single carrier (electronic) and interface limited by Fowler–Nordheim injection.[5] Significant current injection from silicon or commonly used metal electrodes requires electric fields $\gtrsim$5 MV/cm. The trapping probability is several orders of magnitude less than that observed in Si_3N_4 (although any electrons which do get trapped persist as a permanent oxide charge). Despite this, it is only recently that SiO_2 has been seriously considered for TFT applications and has not yet proven to be superior to Si_3N_4. Historically, however, oxide deposited at low temperatures has been far from electronic grade and, although a number of authors have reported various properties of PECVD oxide,[1,2,6,7] there has been no detailed study aimed at optimizing the electrical properties, or reports of oxides with electrical characteristics approaching those deposited by conventional (high-temperature) techniques. In this work we have used the electrical characteristics of metal-oxide-semiconductor (MOS) and metal-oxide-metal (MOM) structures as the primary indication of material quality to develop a process for the deposition of high-quality SiO_2. We have characterized this material using other

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standard techniques and report for the first time a low-temperature oxide with characteristics similar to those deposited at much higher temperatures.

II. EXPERIMENT

The equipment used for thin film deposition was a commerical Plasma Therm PK1250 multiversion system. It has a conventional "radial flow" design and utilizes a mechanical pump/roots blower arrangement for the pumping system. A mixture of 2% SiH_4 in He and pure N_2O were used as the reactive gases and ultra-high purity He was used for additional SiH_4 dilution. Silicon substrates received a standard clean (described, for example, by Irene[8]), and metal substrates (sputtered onto Corning 7059 glass) were degreased before oxide deposition. Most of the Si substrates were degenerately doped (0.001 Ω cm) n-type, although 2-Ω cm substrates were used for C-V measurements. The deposition process variables are described in more detail in the following section. Ellipsometric measurements were made using a Rudolph Research manual ellipsometer, incorporating a mercury discharge lamp as a light source ($\lambda = 5461$ Å), on samples with a thickness corresponding to half an ellipsometric period ($\simeq 1200$ Å). For electrical characterization, Al counter electrodes, typically 500–1000 Å thick with an area of 5.2×10^{-3} cm^2, were evaporated through a shadow mask and the back side of the wafer was etched to ensure good contact. Current-voltage data were taken with a manual voltage ramp in conjunction with a Keithley 26000 logarithmic picoammeter, or with an IBM PC-controlled automated system incorporating a Fluke 3275A power source and a Keithley 619 electrometer/multimeter. Capacitance-voltage data were recorded using a Boonton 71A-SI or 72BD capacitance meter.

III. DEPOSITION PROCESS

A typical PECVD reaction is a complex process, in which many variables must be monitored and/or controlled. Although each of these influences the end result to some degree, it is impractical to optimize each one in a given process. Some of these variables are constrained by equipment design, some are dictated by simple considerations such as uniformity, and others are chosen to tailor certain characteristics of the deposited film. In this work we have used a 13.56-MHz rf power source, the electrode spacing was fixed at 3.2 cm, and the top electrode was maintained at 80 °C. Two different substrate temperatures were used, namely 350 and 275 °C. As we shall discuss later, the most important factor in determining the electrical quality of the deposited material was found to be the rate of deposition. The more important variables which influence this are the total flow of reactive gases, chamber pressure, rf power, and the reactive gas ratio. This ratio R_0 of N_2O to SiH_4 is the primary factor in determining the stoichiometry of the film[9]: silicon oxide films deposited by atmospheric pressure (AP) CVD using $R_0 \lesssim 100$ contain excess silicon, whereas those with $R_0 \gtrsim 100$ have a Si:O ratio corresponding to that of SiO_2. All of the data discussed in this paper were obtained using $R_0 = 125$; the effect of varying R_0 on the film properties will be discussed elsewhere.[10] To vary the deposition rate in a controlled fashion generally requires a change in more than one parameter: For example, increasing the rf power increases the deposition rate but an increase in the reactive gas flow may be necessary to maintain uniformity. Similarly, for a fixed power level, a decrease in the flow rate generally lowers the deposition rate but may require a decrease in chamber pressure for good uniformity. Moreover, the range of deposition rate which is possible using these conventional approaches is usually limited by design constraints. This was certainly the case here, where it proved difficult to obtain good control at low deposition rates. Instead, the approach adopted was to use a high flow of inert "carrier" gas (helium) to ensure uniformity and enable a wide range of deposition rate to be achieved simply by varying the reactive gas flows. The chamber pressure and power level could then be kept constant; 1 Torr and 25 W ($\simeq 0.03$ W/cm^2), respectively, were used for this study. With these parameters the deposition rate was varied in the approximate range of 50–520 Å/min. Details for individual samples are given in Table I.

IV. RESULTS AND DISCUSSION

For insulators which are to be considered for primary insulation purposes, the most important property is the electrical integrity. The interfacial region is clearly an important concern, but equally important are the bulk properties; fixed insulator charge, transient charging, leakage current, and stability are all key issues. Many of these properties can be assessed from simple I-V or C-V characteristics of MOS and MOM structures. For example, much information can be obtained from dynamic ramp-IV characteristics.[11] Curve (A) in Fig. 1 shows such a measurement for an MOS structure where the SiO_2 was deposited at 700 °C by APCVD. For electric fields, $F \lesssim 5$ MV/cm, the displacement current, $I = C\,dV/dt$, dominates (C is capacitance, dV/dt is ramp rate.) The onset of current injection from the silicon substrate occurs at $F \simeq 5$–6 MV/cm, as expected for Fowler–Nordheim injection through the 3.2 eV barrier corresponding to the Si:SiO_2 conduction band discontinuity. The details of the ramp-IV characteristic have been described by DiMaria *et al.*[11] but are basically as follows: As a current flows through the oxide some electrons are captured into deep bulk traps, creating a space charge. At a suitably high current, the charge build-up is enough to significantly affect the electric field at the injecting interface which opposes the ramp voltage and on a logarithmic plot a "trapping ledge" is observed. If all of the traps are filled, or if a dynamic equilibrium is achieved between trapping and high-field detrapping, then the curve may go through the ledge onto a new Fowler–Nordheim characteristic before breakdown. This is a powerful technique as trap parameters such as the capture cross section and capture probability can be determined.[11] This capture probability is related to the current level at which the ledge is observed; the ramp rate and the centroid of the charge distribution.[11] It is approximately 10^{-3} for the as-deposited APCVD oxide which is in good agreement with other APCVD samples.[11] These bulk traps are known to be related to hydrogen or water incorporation[12] and can be re-

TABLE I. Sample identification and description.

Sample ID[a]	Deposition temp. (°C)	Flow rates[b] N_2O:SiH_4:He (sccm)	Deposition rate[c] (Å/min)	Refractive index	Thickness[c] (Å)	Figure no.[d]
9-C	700	APCVD	50	···	1190	1
25-4(A)	700	APCVD	50	···	1330	1
34-C	350	500:200:0	510	1.462	1150	1,2,4
34-D(A)	350	500:200:0	510	1.465	1110	4
57-B	350	200:80:1000	150	1.469	1080	2,3
64-A	350	100:40:2000	60	1.472	1250	2,4,5(a),10
64-B(A)	350	100:40:2000	60	1.464	1280	4
76-B	350	100:40:2000	50	1.471[e]	1570	5(a)
85-B	350	100:40:2000	80	1.471[e]	640	5(a),(b),7
86-A	350	100:40:2000	80	1.471[e]	250	5(a),(b)
68-A	350	100:40:2000	60	1.471[e]	500	6
23-2	700	APCVD	50	···	470	6
85-H	350	100:40:2000	80	···	640	8
76-Nich	350	100:40:2000	50	···	1570	9
65-A	275	100:40:2000	60	1.474	1180	10

[a] Samples marked (A) received a 1000 °C postoxidation anneal in a N_2 atmosphere for 30 min.
[b] The quoted SiH_4 gas flows are those for the 2% SiH_4 in He mixture. That is, 40 sccm corresponds to 0.8 sccm of pure SiH_4.
[c] Deposition rate and thickness are quoted to the nearest 10 Å.
[d] This lists the figures in which data are shown for each particular sample.
[e] Assumed values. For those samples whose thickness was not close to half an ellipsometric period, a noniterative calculation was used to determine the thickness.

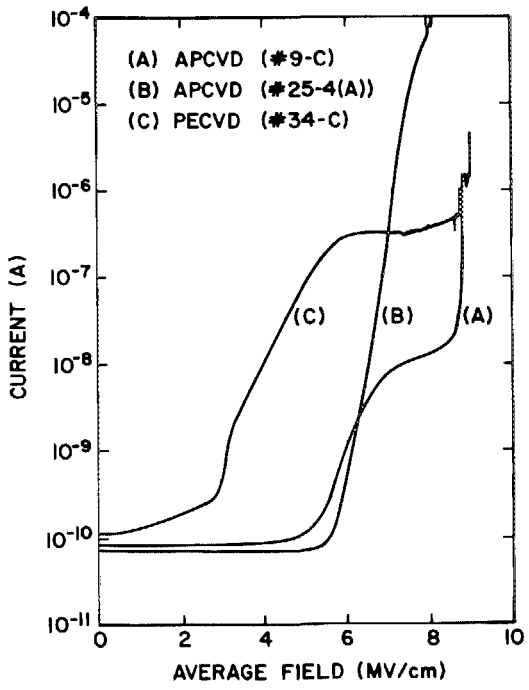


FIG. 1. Ramp-*IV* characteristics for various MOS capacitor structures: (A) APCVD oxide deposited at 700 °C. (B) Similar APCVD oxide annealed at 1000 °C for 30 min in a N_2 atmosphere. (C) PECVD oxide deposited at 350 °C using a typical process (see Table I for details). In all cases the ramp rate was ~0.5 V/s in the positive bias direction, corresponding to electron injection from the silicon substrate.

duced by a high-temperature anneal. Curve (B) in Fig. 1 shows a similar APCVD sample which received a post oxidation anneal (POA) at 1000 °C for 30 min in a N_2 atmosphere. The characteristic displays the same features as the unannealed sample except that the trapping ledge occurs at a higher current level. As expected, the trapping probability has been decreased and the characteristic resembles that of thermally grown SiO_2. In contrast, curve (C) shows a ramp-*IV* characteristic for a PECVD sample deposited at 350 °C by a standard process. This process was essentially that described in Sec. III but using only the 2% SiH_4 in He and N_2O gases. The flow rates were high enough to ensure uniformity (see Table I for details), and resulted in a deposition rate of $\simeq$510 Å/min. The electrical integrity of this oxide is very poor. Premature current injection occurs at very low fields, less than 1 MV/cm in this case, and it is meaningless to try to extract any trap information. The characteristics, although highly reproducible both across a given wafer and between wafers from the same deposition run, were not reproducible from run to run and the extent of premature injection varied greatly, even between runs with identical process variables. However, these features are a strong function of the rate of film deposition and this aspect is discussed in Sec. IV A.

A. The effect of deposition rate on oxide properties

1. Electrical characteristics

Figure 2 shows the effect of deposition rate on the ramp-*IV* characteristics. These data were obtained for samples de-

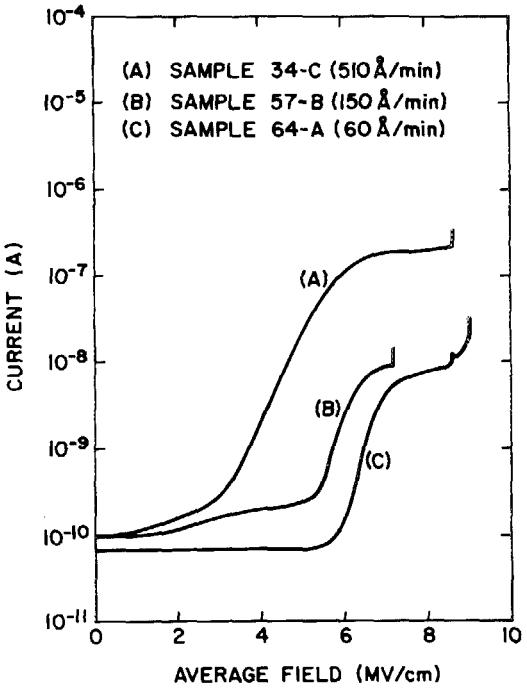


FIG. 2. The effect of deposition rate on the ramp-IV characteristics. The ramp rate was ~0.5 V/s and the voltage polarity was positive.

posited at 350 °C using the various flow rates described in Table I. As the flow of reactive gases was decreased to lower the deposition rate, the carrier flow was increased to achieve uniformity. All of the other variables were held constant, as described in Sec. III. The data in Fig. 2 illustrate the trend observed throughout this work of an improvement in the electrical integrity with decreasing deposition rate: The reproducibility improves, the premature injection is reduced, and the breakdown field increases. Although the positive bias case (injection from the Si substrate) is shown in Fig. 2, the extent of premature injection was largely independent of the bias polarity. When the deposition rate is lowered sufficiently, the characteristics become close to ideal and reproducibility is excellent. In this work we found that a rate $\lesssim 80$ Å/min was necessary, although this is likely to depend strongly on the details of the PECVD system and process used. Note that curve (C) in Fig. 2 closely resembles the APCVD sample [curve (A) in Fig. 1], and exhibits no significant current injection for fields $\lesssim 5$–6 MV/cm.

The origin of this premature injection exhibited by oxides deposited at high deposition rates is unclear at this time, although a number of experimental observations give some insight. The possibility of a Si-rich region giving enhanced injection can be eliminated by noting that the problem occurs under both voltage polarities, that is injection from the Si substrate and the metal gate. It is possible to envision a Si-rich region at the first interface during an initial plasma transient, but this would not be expected for the second interface unless the whole oxide was Si rich. This is not the case in the films studied here as both the ellipsometry and RBS data (described below) would detect significant deviations from stoichiometry. The most probable explanation is that the interfaces are nonplanar, giving rise to regions of high electric field which causes enhanced injection—very similar to the effect of rough poly-Si in MOS memory technology.[13] Figure 3 shows the effect of successive voltage ramps on the I-V characteristic of sample (B) in Fig. 2. After the first ramp, the degree of premature injection is greatly reduced and the characteristic improves. In fact, the second ramp closely resembles that of a good oxide and exhibits the usual permanent charge trapping in subsequent ramps. This is typical of localized injection due to asperities or microscopic thickness fluctuations at the injecting interface—the improvement after the first ramp resulting from electron trapping in the oxide.[14] The large current density injected at local high-field regions causes a permanent trapped space charge which screens and "seals" the injection point, minimizing premature injection in successive ramps. The good reproducibility exhibited between contacts on a given wafer indicates that the injection must be microscopic on the scale of the contact area and thus appears to be uniform across the sample.

2. Film stoichiometry

The refractive index measured by ellipsometry can be used to detect deviations from stoichiometry in good quality oxide. However, the quoted range for "stoichiometric" SiO_2 deposited by PECVD is large (1.46–1.52) and this must result from some differences in stoichiometry. Data for oxides deposited by the various processes used here are summarized in Table II. (The refractive indices are mean values, determined from a number of samples from different deposition runs, and the standard deviation is quoted as the uncertainty.) First we discuss the as-deposited films, the effect of annealing will be discussed later. The experimental scatter is greatest for those oxides deposited rapidly (consistent with the electrical data), but it is still very small. Also, there is a small but distinguishable difference between the refractive indices of films deposited rapidly and slowly, although both are close to that of thermal oxide (1.465). However, many factors influence refractive index[16] and comparisons are

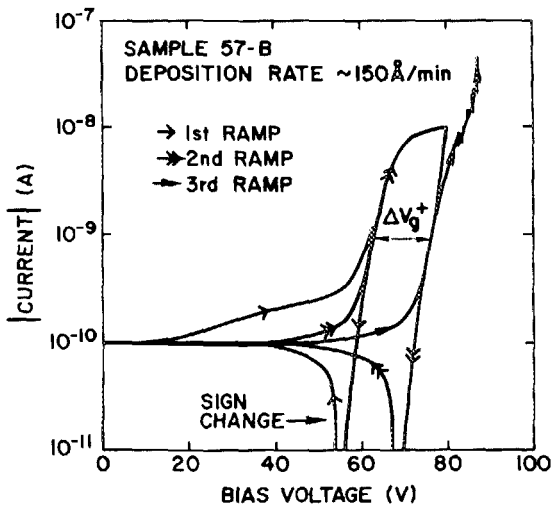


FIG. 3. The effect of consecutive voltage ramps on the characteristic of MOS structures exhibiting premature injection. The ramp rate was ~0.5 V/s and the voltage polarity was positive. The voltage shift, ΔV_g^+ is due to permanent electron trapping in the oxide bulk.

TABLE II. Oxide properties.

Sample type	Deposition temp. (°C)	Av. dep. rate (Å/min)	Anneal (POA)[a]	Refractive index[b]	Thickness change (%)	Si:O ratio[c]	Etch rate[d] (Å/s)
Slow	350	60		1.471(± 0.001)	···	33.7:66.3	8.1
Slow	350	60	✓	1.463(± 0.002)	< 1[e]	···	2.5
Slow	275	60		1.473(± 0.002)	···	33.7:66.3	8.9
Slow	275	60	✓	1.463(± 0.002)	< 1[e]	···	···
Fast	350	520		1.467(± 0.004)	···	32.6:67.4	16.2
Fast	350	520	✓	1.463(± 0.003)	− 4	···	2.5
APCVD	700	50		1.444(± 0.001)	···	33.1:66.9	9.0
APCVD	700	50	✓	1.454(± 0.001)	···	···	···
Thermal	1150[f]	···		~ 1.465	···	33.3:66.7	2.0

[a] 1000 °C in a N_2 atmosphere for 30 min.
[b] The quoted errors are the standard deviations obtained from measurements on samples from a number of different deposition runs. All samples were approximately half an ellipsometric period in thickness.
[c] Measured using Rutherford backscattering spectroscopy (RBS).
[d] Measured using "P" etch (see Ref. 16 and text).
[e] These samples always showed a small *increase* in the measured thickness.
[f] Growth temperature.

only meaningful when supported by other data. Similarly, the small differences between the various oxides detailed in Table II are difficult to interpret and this will not be attempted here. We do know, however, that they are not silicon rich, since as little as 1% excess silicon in these oxides can easily be detected by ellipsometry.[10]

In contrast, solid-phase analysis techniques can give a direct measurement of film stoichiometry and, in extreme cases, impurity content. Table II lists the Si:O ratio determined by Rutherford backscattering spectroscopy (RBS) for films deposited by various processes. All of the oxides measured had a Si:O ratio close to that expected for stoichiometric SiO_2, particularly those samples which were deposited slowly (at both 350 and 275 °C). The sample which was deposited rapidly was, if anything, slightly silicon deficient. No impurities were detected in any of the oxides, although the sensitivity was low and hydrogen (the most likely impurity) would not be detected in any case. However, we know that the hydrogen content is very low (compared to typical PECVD oxides) from IR absorption data. These measurements (on samples $\simeq 1\,\mu$m thick) gave a hydrogen concentration of ~ 1 at. %, which was incorporated as Si–OH with no detectable Si–H present (detection limit ~0.1 at. %). These data are in qualitative agreement with the findings of Pai *et al.*[17] where helium dilution of the reactive gases was shown to have a profound effect on the incorporation of hydrogen in SiO_x films. In addition to the IR data, a preliminary comparison between APCVD and slowly deposited PECVD material by the nuclear reaction analysis technique revealed a lower hydrogen concentration in the PECVD oxide. Actually, this is of secondary importance from the viewpoint of electrical integrity, where the concern is the number of electrically active defects and this can be determined from ramp-*IV* measurements.

3. Etching rate

Oxides deposited by various techniques differ in their resistance to certain etchants. One very sensitive etchant which has been used successfully in the past is "P" etch.[16] According to Ref. 16, this etches porous (sputtered) SiO_2 at 20–70 Å/min, APCVD oxide at $\simeq$ 13 Å/min, and thermally grown oxide at $\simeq$ 2 Å/min. This solution, 15 HF (40%):10 HNO_3(70%):300 H_2O, was used to determine the etching rates for the various oxides discussed above and the results are shown in Table II. The data are in general agreement with those contained in Ref. 16: The thermal oxide etched very slowly ($\lesssim$ 2 Å/min), the APCVD sample somewhat faster ($\simeq$ 9 Å/min) and the PECVD oxides deposited by our standard process etched relatively quickly ($\simeq$ 16 Å/min). However, the significant result is that the PECVD oxides which were deposited slowly had approximately the same etching rate as the APCVD samples, suggesting that their composition may be similar. We shall return to this point in the following section when the electrical characteristics of the two oxides are compared.

Further information regarding the structure of oxides deposited at different rates can be obtained by examining the effect of a high-temperature anneal on the film properties. Table II also summarizes the ellipsometry data obtained on samples which were given a 1000 °C anneal in N_2 for 30 min. Films which initially have poor electrical characteristics (those deposited using high rates) densify after annealing: The film thickness decreases by $\simeq$ 4% on average, although the value measured for the refractive index is not significantly different. Such a densification has been reported previously for insulators deposited using low temperature techniques[15] and is often considered to be usual. However, films which exhibit good electrical characteristics (those deposit-

ed slowly) do not change significantly in thickness, although the refractive index decreases slightly. The corresponding ramp-*IV* characteristics are shown in Fig. 4. For samples with initially good characteristics the main effect of annealing is reduced trapping, similar to that observed with APCVD samples (Fig. 1) and as expected for a good quality oxide. In contrast, the characteristic for the poor oxide changes significantly: There is a large reduction in the degree of premature injection and the general shape of the curve more closely resembles a typical oxide, although there are many low-field (nonshorting) breakdown occurrences which would be destructive in actual devices. This is consistent with the densification noted from the ellipsometry data and also with the etching rate data shown in Table II. After anneal, both the rapidly and slowly deposited oxides have an etching rate close to that of thermal SiO_2, although the change is much greater in the initially porous oxides.

The observations discussed in this section give some insight into the structure of the poor-quality films. They are certainly less dense than high-quality oxides, the deposition rate being too high to allow the formation of a uniform dense SiO_2 layer, and are porous in nature. Films with such poor bulk properties are likely to form nonplanar interfaces which would enhance current injection, and in the worst cases may even give rise to conduction along bulk leakage paths through micropores. The decrease in premature injection upon densification by high-temperature annealing supports this view. It is clear from the preceding discussion that the ramp-*IV* measurement is very sensitive to subtle changes in the oxide layers—much more so than the RBS or ellipsometry measurements. However, these latter techniques are macroscopic and give no indication of the microscopic structure of the material. Information on atomic structure, such as bonding or suboxide formation, can be obtained from other, largely spectroscopic techniques.[16,17] On the other hand, the etching rate is also very sensitive to the differences between the various oxide layers and in this respect, supports the electrical data. However, the most important assessment of a potential gate insulator must be the electrical integrity. The poor quality oxides are far from ideal for use as primary insulators, even in *a*-Si:H TFTs, where the requirements are not very stringent. The oxides deposited at the highest deposited rates, although nominally SiO_2, do not behave so electrically. In addition to the features already described, the trapping characteristics are atypical: Repeated ramp-*IV* measurements show that a portion of the oxide charge is reversible, somewhat reminiscent of an oxynitride layer. The premature injection in all but the slowest deposited films gives rise to significant gate current and charge trapping at typical gate voltages and would result in threshold voltage shifts in actual devices. With Si_3N_4 as the gate dielectric, one expects charge trapping and associated problems during operation,[18] but in this case the charge state of the insulator can be neutralized by maintaining an opposite gate bias during the "off" cycle.[19] With SiO_2, the trapping is essentially permanent and gate leakage cannot be tolerated. However, in high-quality oxide there is no gate current at typical operating voltages and stability is expected to be much better in oxide-based structures. In the following section we discuss the electrical characteristics of the slowly deposited films in more detail, and assess their potential for use as a gate material in TFT structures.

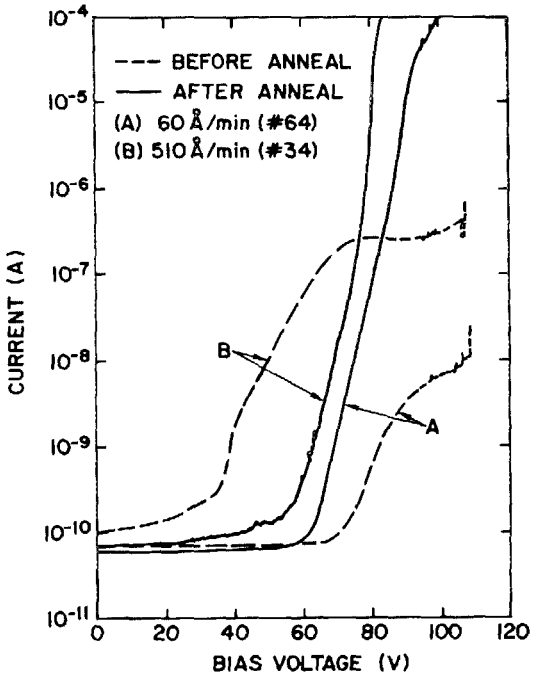
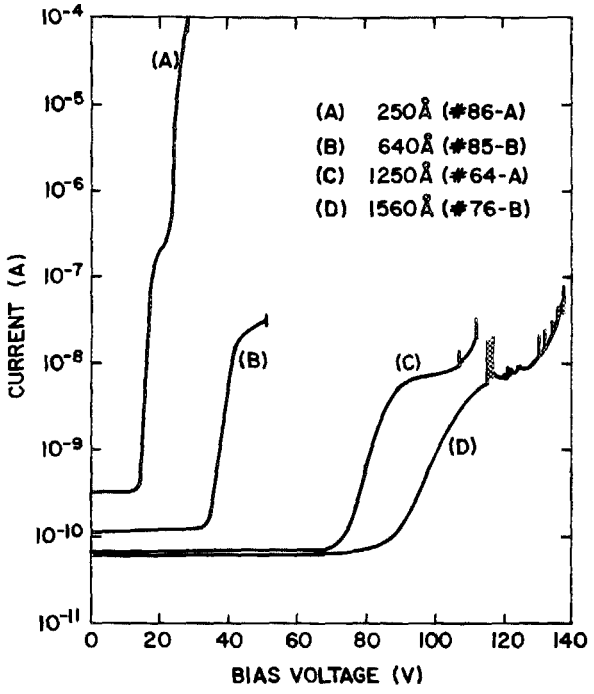


FIG. 4. The effect of high-temperature anneal on ramp-*IV* characteristics. The characteristics before and after anneal (1000 °C for 30 min in N_2) are shown for oxides deposited using both low and high deposition rates. The ramp rate was 0.5 V/s and the voltage polarity was negative.

B. Electrical characterization of oxide deposited using low deposition rates

Figure 5(a) shows the ramp-*IV* characteristics for a number of samples with various oxide thicknesses in the range 250–1570 Å. These samples were all deposited under identical conditions at a low rate. The voltage at which current injection occurs scales with oxide thickness and corresponds to a field of $\simeq$5–6 MV/cm. Also, the current level at which the trapping ledge is observed decreases with increasing thickness, as expected[11]: The deep traps responsible for the trapping ledge are bulk traps and consequently the electron trapping decreases with thickness. It is evident from the data shown in Fig. 5(a) that good characteristics can be obtained over a wide range of oxide thickness. The slow deposition makes it possible to deposit very thin films with good electrical integrity ($\lesssim$ 50 Å can be deposited routinely, although this ultrathin regime will not be discussed here). Figure 5(b) shows a standard Fowler–Nordheim plot of *I-V* data obtained from sample no. 86-A [curve (A) in Fig. 5(a)]. These data were taken in pulsed mode to minimize the effect of electron trapping, enabling the true Fowler–Nordheim characteristic to be measured over a wide current range. The linearity of the plot is good, and the data are well described by the simple Fowler–Nordheim expression given in the figure. The barrier height ϕ (approximately equal to the $Si:SiO_2$ conduction band discontinuity) was determined to be $\simeq$3.2 eV, in good agreement with the accepted value.

Figure 6 shows a direct comparison, between the ramp-*IV* characteristics of similar samples deposited by APCVD



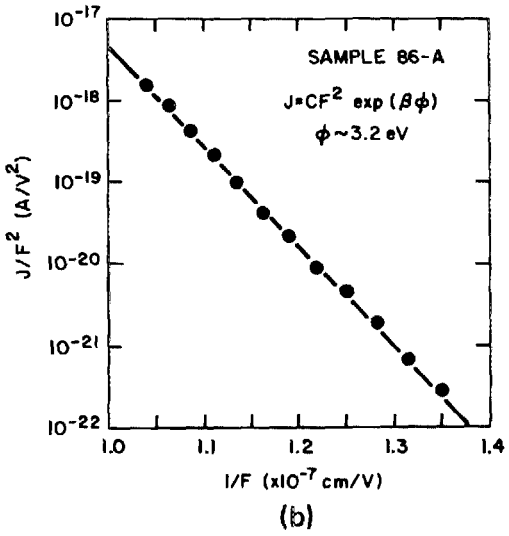


FIG. 5. (a) Ramp-*IV* characteristics for MOS capacitors fabricated with various oxide thicknesses. All of the oxides were deposited using a low deposition rate at a temperature of 350 °C. The ramp rate was ~0.5 V/s and the voltage polarity was positive. (b) Fowler–Nordheim plot of *I-V* data from sample 86-A. The barrier height ϕ was determined from the slope of the plot, assuming an effective mass m^* of 0.5 m.

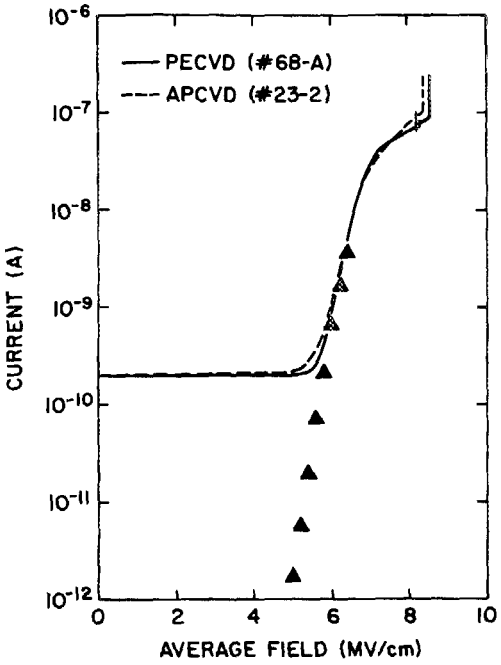


FIG. 6. Comparison between the ramp-*IV* characteristics of a PECVD sample deposited at 350 °C and an APCVD sample deposited at 700 °C. In both cases the oxide thickness was ~500 Å. The ramp rate was 0.5 V/s in the positive bias direction. The data points are from a point-by-point measurement on the PECVD sample in order to eliminate the displacement current.

and PECVD at 700 and 350 °C, respectively. The two curves are virtually identical; current injection occurs at approximately the same field and the trapping ledge is observed at the same current level. This indicates that the density of the deep, water-related traps is approximately the same in both samples, despite the fact that they were deposited at very different substrate temperatures. The discrete data are a point-by-point *I-V* measurement for the PECVD sample and demonstrate that no significant current flows for fields $\lesssim 5$ MV/cm. Another important parameter in the assessment of the low-temperature oxide is the breakdown field. In all of the curves shown in Fig. 5(a) the average oxide field at which destructive breakdown occurred (F_{bd}) was ~10 MV/cm, although there was a trend of increasing F_{bd} with decreasing oxide thickness. This effect can also be related to charge trapping in the oxide.[14] The thicker films trap more electrons before breaking down which means that the maximum field in the oxide (the anode field) is significantly higher than the average field. Quoting F_{bd} for individual capacitors is not really meaningful and usually many capacitors are measured to give a statistical distribution. Figure 7 shows such a distribution for a 640-Å-thick oxide, where 80 capacitors, each with an area of 5.2×10^{-3} cm^2 were stressed to breakdown. The voltage polarity for this test was positive, that is electron injection from the silicon substrate. The distribution is very narrow, peaked at an average oxide field of 8–9 MV/cm and there are no shorted capacitors or low field breakdowns. As discussed above, charge trapping in the oxide can result in significant differences between the maximum (anode) field and the average field. The anode field at breakdown was estimated[11] to be ~12 MV/cm [note that in the thinnest sample shown in Fig. 5(a) the *average* field at breakdown is $\simeq$12 MV/cm]. These results are very respectable, even when compared with thermally grown oxides, and were obtained from samples prepared under ordinary laboratory (nonclean) conditions.

The properties which have been discussed so far, compare favorably with oxides deposited by APCVD at a much higher temperature. However, these are largely bulk properties and the electronic behavior of the Si:SiO$_2$ interface have been ignored until now. The plasma-assisted process, although low temperature, is not a low-energy one and interfacial damage is to be expected. Figure 8 shows *C-V* data for an

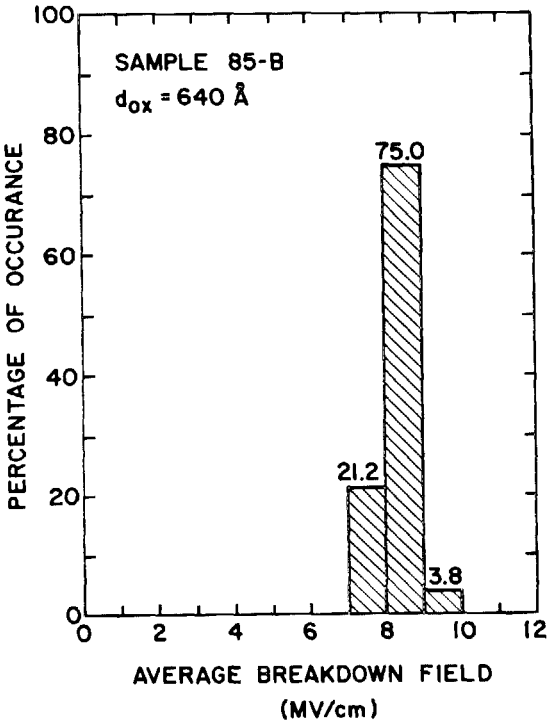


FIG. 7. Histogram showing the relative number of capacitors as a function of average oxide field at breakdown. To obtain this, 80 capacitors, each with an area of 5.2×10^{-3} cm^2, were ranged with a constant current source to breakdown. The test polarity was positive corresponding to injection from the silicon substrate.

MOS capacitor fabricated on a 2-Ω cm silicon substrate. The solid curve shows the high-frequency characteristic for an as-deposited sample. Initially there is a flatband voltage shift of $\simeq -1$ V, which increases upon ramping into depletion. After this initial shift, the C-V curve exhibits a small amount of hysteresis—the direction of which is indicative of interface states rather than mobile ion drift. In addition to this there is a large amount of "stretch out" due to interface states, from which an interface state density of $\simeq 1\times10^{12}$ cm^{-2} eV^{-1} was deduced.[20] Although this is high it is not much greater than that measured in as-grown thermally oxidized samples. As is the case with conventional oxides,[21] the interface damage is reduced dramatically by a postmetallization anneal (PMA). The dashed curve in Fig. 8 shows the C-V characteristic of the same sample after a PMA in forming gas (10% H_2 in N_2) at 400 °C for 30 min. The stretch out and hysteresis have been virtually eliminated. Comparison with the low-frequency (quasistatic) characteristic (the dotted curve) shows that the interface state density is very low (estimated to be $\sim4\times10^{10}$ cm^{-2} eV^{-1} in this case). Again, these data are very respectable, even when compared with thermally grown oxides, although obviously not "state of the art." However, it is the bulk properties of the oxide, as well as the Si:SiO_2 interface that is at issue here and there are many applications for high-quality, low-temperature insulating layers where the interfacial role is secondary. One such example is in a-Si:H based TFTs, where the interface is formed from a-Si:H and an insulator, both of which are deposited by PECVD. To date, the poor bulk properties of the low-temperature insulators have prevented the interface from becoming a key issue. A study of the amorphous silicon–silicon dioxide interface is outside the scope of this paper, and in the remainder of this section we concentrate on demonstrating that the bulk electrical properties surpass those required for a-Si:H TFTs.

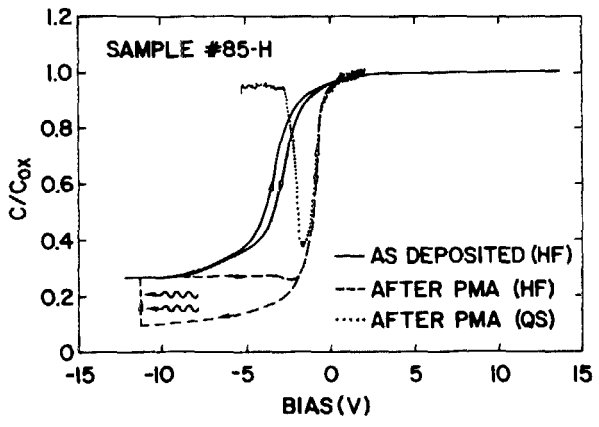


FIG. 8. Capacitance-voltage characteristics for MOS capacitors fabricated on 2-Ω cm silicon substrates. The oxide was deposited at 350 °C using a low deposition rate. The solid curve is the high-frequency (1 MHz) characteristic for a sample with an as-deposited oxide. The dashed curve was measured on the same sample after a 30-min postmetal anneal in forming gas at 400 °C. After ramping the sample into deep depletion (ramp rate $\simeq$0.5 V/s), the inversion layer was formed by illumination before returning to accumulation. The dotted curve is the quasistatic C-V characteristic (after anneal) taken using a ramp rate of $\sim$50 mV/s.

There are two basic TFT structures—"normal" where the a-Si:H is deposited first, followed by the insulator, and "inverted" where the insulator is deposited directly onto the gate metal, before the a-Si:H layer. For this latter structure it must be possible to deposit high-quality material directly onto a (polycrystalline) metal substrate. To test this, MOM structures were fabricated and characterized. Molybdenum and nichrome substrates (sputtered films on glass) were used, and gate electrodes were aluminum, as usual. Figure 9 shows I-V characteristics, both ramped and point by point, for typical MOM capacitors. Each characteristic was taken on a virgin dot to eliminate the effect of charge trapping at high fields. The ramp-IV characteristics are essentially identical to those obtained using MOS structures except that Fowler–Nordheim injection occurs at slightly higher fields under positive gate bias, reflecting the small difference in work function between n^+ silicon and nichrome. Similar results were obtained with molybdenum substrates except in that case the oxide broke down ($F_{av}\simeq$8–9 MV/cm) before significant current injection was observed under positive bias. The point-by-point measurement in Fig. 9 eliminates the displacement current at low fields and it is clear that the leakage current in these structures is essentially zero for fields $\lesssim$5 MV/cm. This means that for typical TFT operating voltages ($\lesssim$20 V), 1000 Å of oxide is more than sufficient as a gate dielectric. The absence of low field breakdowns (see, for example, Fig. 7) indicates that pinholes and gross defects should not be a problem. With a poor-quality oxide, such as those deposited at high deposition rates, several thousand angstroms of material would be necessary to minimize gate leakage and gradual charging of the oxide would be a long-term stability problem.

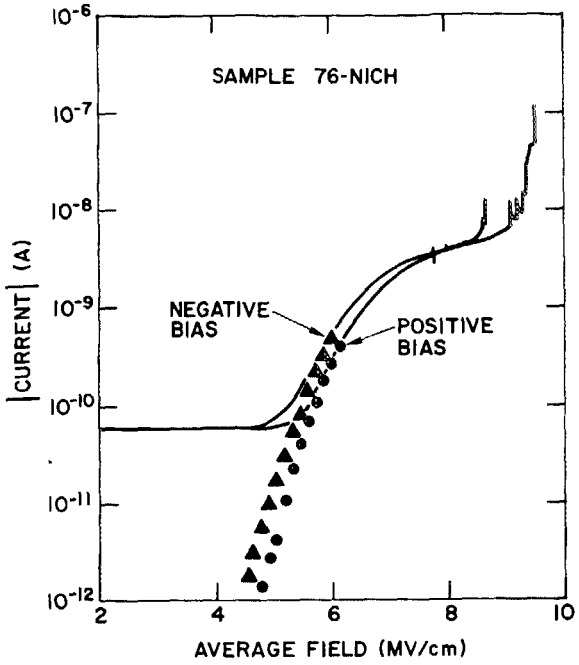


FIG. 9. *I-V* characteristics for MOM capacitors. The oxide was deposited at 50 Å/min using a substrate temperature of 350 °C onto nichrome on glass substrates. The counter electrodes were aluminum. The ramp was 0.5 V/s for the ramp-*IV* measurement and the point-by-point data were taken to eliminate the displacement current.

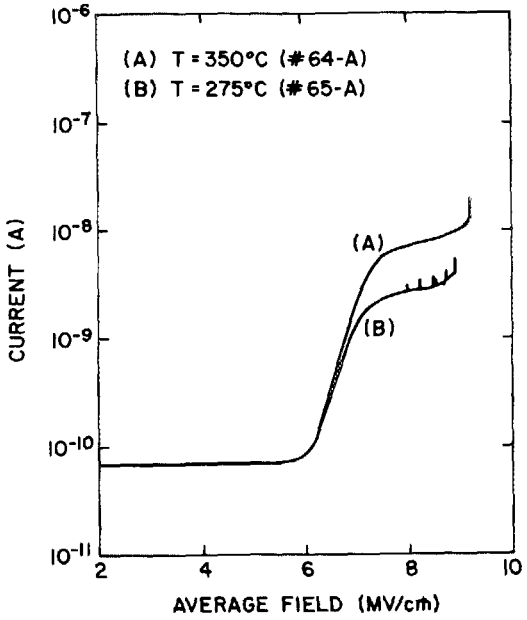


FIG. 10. The effect of substrate temperature on (MOS) ramp-*IV* characteristics. Other than substrate temperature, the process variables were the same in both cases and the oxide deposition rate was 60 Å/min. Note the increased electron trapping in the oxide deposited at the lower temperature (275 °C).

Another important difference between the normal and inverted structures is one of deposition temperature. In inverted structures the maximum deposition temperature is dictated by the properties of the glass substrate, and the temperature used here (350 °C) is below the softening temperature for borasilicate glasses. However, in noninverted structures the properties of the *a*-Si:H layer dictate this temperature since its electronic properties are altered by temperatures much in excess of 275 °C. For this reason, we have also assessed the properties of oxides deposited at 275 °C. The results are very similar to those obtained at 350 °C. Fast deposition results in electrically poor oxides, whereas those deposited slowly are stoichiometric (as far as RBS and ellipsometry measurements indicate–see Table II), etch at approximately the same rate (also Table II), and have good electrical characteristics. Figure 10 shows ramp-*IV* characteristics for similar MOS structures deposited at the two temperatures. The two curves show similar characteristics and Fowler–Nordheim injection occurs at approximately the same field in both cases. The only significant difference concerns the position of the trapping ledge. It occurs at a lower current level in the 275 °C oxide indicating an increase in the trapping probability (and hence the density of electrically active defects) by a factor of ~5. This is significant, although it would only be a problem in an actual device if electrons were introduced into the oxide conduction band during operation. We know from the measurements presented here that leakage current should not be a concern and the problem of hot electron transfer from the channel, which is a serious one in MOSFET technology, should not exist in the low-mobility *a*-Si:H-based structures.

V. CONCLUSIONS

High-quality silicon dioxide has been deposited at very low substrate temperatures by PECVD. The film properties were found to depend strongly on the deposition rate, with a low rate ($\lesssim 80$ Å/min) being essential for obtaining good-quality material. Control over the rate of deposition was achieved by using very low reactive gas flows, together with a much higher flow of inert carrier gas to ensure uniformity. Films deposited at conventional high rates (~510 Å/min) are of a much lower quality: Although still "stoichiometric" (as determined by ellipsometry and RBS), they are porous and have poor electrical characteristics, exhibiting premature injection at low electric fields. The properties of films deposited very slowly (~60 Å/min) at 350 °C compare favorably with those of SiO_2 deposited by APCVD at 700 °C. They are relatively dense, essentially pinhole-free, exhibit good electrical integrity, and can be deposited in very thin layers as a result of the low deposition rate. Material deposited at 275 °C also has good electrical characteristics, although exhibits increased electron trapping. Either temperature can be used to deposit onto metal substrates without deteriorating the film properties. These two latter points are important considerations for *a*-Si:H TFT applications.

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