HIGH EFFICIENCY SELECTIVE EMITTER CELLS USING IN-SITU PATTERNED ION IMPLANTATION

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ABSTRACT: In this paper, we introduce a novel manufacturing process flow for cost effective mass production of high efficiency solar cells enabled via "in-situ patterned" ion-implantation. This novel doping approach has several advantages over diffusion based alternatives 1) Simplification of the process flow by eliminating the non-value add steps such as PSG strip and junction isolation, 2) Superior junction quality through precise dose control 3) Improved surface passivation using thermal oxide growth and 4) Patterned doping required for highest efficiency cells. As an example of the application of patterned ion implantation, we discus the Solion "Blue" process for the fabrication of phosphorus doped selective emitters on 156mm p-type Cz wafers that enables the production of >18.5% efficiency solar cells (*higher Watts*) with simplified processing (*lower processing Cost)*. The tighter binning and higher performance achieved with this process makes a compelling case for patterned ion implantation as the preferred doping approach for selective emitter cells and provides a roadmap for other high efficiency cell structures.
Keywords: Ion Implantation, Selective Emitter, High Efficiency

1 INTRODUCTION

There has been a rapid growth in the photovoltaics (PV) industry in the recent years largely driven by the government offered incentives [1] The key objective for the PV industry to sustain this growth without any incentives is to achieve grid parity This increased demand for PV is also fueling new innovations in manufacturing technology focused on enabling higher performance at a lower conversion cost. Improvements in cell efficiency are extremely valuable towards the goal of reaching grid parity since the cost improvements are leveraged across the entire value chain, from reducing the grams of silicon used per watt to reducing the process costs/watt to reducing the total number of modules required for the final installation. Technologies that simplify solar cell manufacturing and improve the cell efficiencies will have a strong future in PV.

While there are a couple of cell architectures in mass production that have cell efficiencies exceeding 20%, such as the interdigitated backside contact (IBC) cells (Sunpower Corp) or the HIT cells (Sanyo), the majority of cells in mass production today are based on a homogenous frontside emitter on p-type Si substrates using a $POCl_3$ diffusion process. The doping level in emitter layer on the frontside of the cells plays a critical role in determining the cell performance. While lightly doped emitters (higher Rsheet) are needed for reducing the carrier recombination in emitter, a high surface concentration is needed to make low resistance contacts with the metal lines. This tradeoff is resolved in the selective emitter cell architecture where the emitter is heavily doped only under the metal contact regions and lightly doped in other regions to reduce carrier recombination in the emitter and thus improve the "blue" response of the cells. The selective emitter cell architecture is the next logical step towards higher cell efficiencies on standard p-Si cells [2]. Even though there are several commercially available selective emitter manufacturing solutions [3-7], there is no clear winner. It is important to note the winning technology solution will be one that provides the versatility to enable advanced cell structures beyond the selective emitter on p-type Si substrates and enables a roadmap to grid parity.

In this paper we present the benefits of precision patterned ion implantation in enabling high efficiency selective emitter cells on p-Si substrates. Ion implantation is a process of precisely introducing a known amount of energetic particles into any substrate to alter its material properties. This is mature and proven technology used extensively in integrated chip manufacturing due to the precision doping requirements of fabricating billions of transistors on each semiconductor wafer [8]. Ion implantation has previously been utilized in the fabrication of high efficiency Silicon solar cells on both p and n-type Si substrates [9, 10], however the commercial viability of this technology is being re-enabled through advancements in both the implantation equipment and other steps in cell manufacturing. The key innovation in this ion implantation technology is precision patterned doping in a single ion implantation process utilizing VSEA's proprietary in-situ masking technology [11] at the high throughputs needed for low cost of manufacturing. The practical implementation of this technology is demonstrated via the fabrication of selective emitter cells using patterned implantation of phosphorous on p-type Si substrates resulting in improved cell efficiency from a $POCl_3$ based baseline of 17.5% to >18.5% (average) with ion implanted selective emitters. It is evident that the versatility of patterned ion implantation will be instrumental in enabling the fabrication of higher efficiency structures on both p and n-Si

2 TECHNOLOGY REQUIREMENTS

To evaluate the advantages of ion implantation as an alternative doping technology to diffusion, we compare the following attributes of our approach to a standard diffusion based manufacturing process flow,

1) Process Simplification
2) Superior Junction Quality
3) Improved Surface passivation
4) Integrated Patterned Doping

We also note that all the alternative selective emitter

processes based on diffusion will require additional steps to create the selectively doped regions and hence will add cost to the standard process.

2.1 Process simplification

Figure 1 compares the standard $POCl_3$ homogeneous emitter process flow [12] to VSEA's Solion "Blue" process flow for p-type mono-crystalline wafers. The as-cut wafers in both process flows go through conventional saw damage etch and KOH/IPA texture to form random upright pyramids. In the standard $POCl_3$ process, the wafers go through a diffusion furnace to create a homogeneous emitter with a sheet resistance of 50-60 Ohm/sq. This diffusion process comprises of multiple steps in the recipe including pre-oxidation, phospho-silicate glass (PSG) deposition, phosphorus drive-in step and post oxidation steps and requires elaborate process optimization of the operating pressure, gas flowrates, duration of multiple species and careful hardware design to obtain a repeatable performance needed for high volume manufacturing.

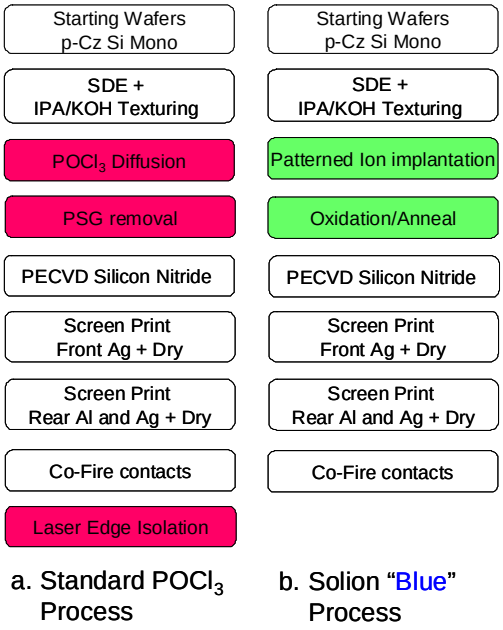

Figure 1. Process simplification for fabrication of Selective emitter cells using ion implantation. The Solion "Blue" process simplifies processing by eliminating complex diffusion recipes, the PSG removal wet etch step as well as the junction isolation step.

The PSG layer in a $POCl_3$ diffusion process deposits on the entire wafer surface and thus results in a parasitic emitter on the backside of the wafers. Since both the PSG layer and parasitic emitter have to be removed to have high efficiency cells, this process adds two non-value add steps (PSG strip and junction isolation step) in the process flow adding to the cost of manufacturing these cells.

The patterned doping in VSEA's Solion "Blue" process is accomplished through the use of an in-situ proximity mask introduced during the implant step to selectively dope only the frontside of the wafers [11]. This doping approach is unique in that the dopant atoms are directly introduced into the silicon lattice without any external film deposited on the surface that may require removal in subsequent steps. The directional nature of ion implantation process ensures only the surface exposed to the energetic ions gets doped hence enabling single side doping which is critical for the advanced cell structures. Single sided doping eliminates the formation of a parasitic emitter making the junction isolation step redundant in our process. The wafers are then annealed in a furnace activate the implanted dopants. A thin thermal oxide is also grown in during the anneal process providing excellent passivation of the emitter. The anneal recipe used here is extremely simple compared to the standard $POCl_3$ recipes with the oxide thickness easily controlled via the oxidation time during the process. Typical process temperatures (800-900^oC for 10-60min) as used in $POCl_3$ recipes are sufficient to activate the implanted dopant as well as passivate the emitters.

Following the doping steps, the wafers get a thin (optimized) antireflective coating of SiNx films. A thinner nitride layer is need for the implanted emitters due to the presence of the thin oxide on the surface. This has an added advantage for improving the productivity of the SiNx tool. The front and backside metal contacts are then screen printed, dried and fired using standard screen printing processes in both process flows. Standard $POCl_3$ based cells go through a laser junction isolation step to complete the process flow while the implanted cells do not require this isolation step as mentioned previously.

The Solion "Blue" process removes a total of two existing processing steps from the standard manufacturing sequence while adding just the implant step to the sequence. For selective emitters, the net reduction of process steps is even higher since all alternative diffusion based SE process flows add more steps to enable patterned doping to the standard diffusion process flow while patterned doping is integrated into the Solion "Blue" process. Ion implantation also eliminates any wet processing steps (post texturing) and thus enabling "dry" processing of the wafers which is desirable to reduce the wet-chemical waste treatment costs from the manufacturing facility. The Solion "Blue" process thus requires fewer steps than any diffusion based process flows, enables oxide passivation of the emitter, improves productivity of the nitride tool and enables dry processing.

2.2 Superior Junction Quality

The poor across wafer and cross batch uniformity of this process is controlled by the uniformity of composition and thickness of the deposited glass layer (that acts as the dopant source for the wafer) and has limited the cell manufacturers from going to higher Rsheet emitters, whence uniformity of the dopant profiles becomes a critical factor in having a repeatable contact performance across the entire wafer surface.

Ion implantation provides a powerful method to precisely control the amount of dopant in the emitter layer. The dopant profile may thus be using the appropriate anneals to maximize cell performance. Precise profile control eliminates the dead layer associated with diffused emitters. The uniformity and precision doping via implant enables a repeatable process for fabrication of lightly doped emitter regions [11-13]. For the same sheet resistance the implanted emitters have a lower surface concentration than diffused emitters thus enabling lower recombination in the emitters

One concern about the implant process is if the implanted regions can be perfectly regrown without any

residual damage in the implanted layer. Defects in the regrown lattice may cause increased carrier recombination in the emitter. Figure 2 shows a TEM comparison of implanted and diffused emitters with similar Rsheet values of 60ohms/sq. The cross-section comparisons illustrate the perfectly regrown Si crystal lattice with no dead regions in the near surface regions of the implanted emitter. The image also illustrates the presence of a thin layer of thermally grown silicon dioxide layer during the post-implantation anneal used for regrowth of the crystal and activation of the implanted dopants. The smoother interface between the oxide layer and the Si sample for the implanted emitters (reduced surface recombination area) combined with the high quality thermal oxide (with very few interface states) is also evident in the picture. This smooth interface is partly responsible for excellent passivation of the emitter and results in reduced surface recombination essential for high efficiency selective emitter cells.

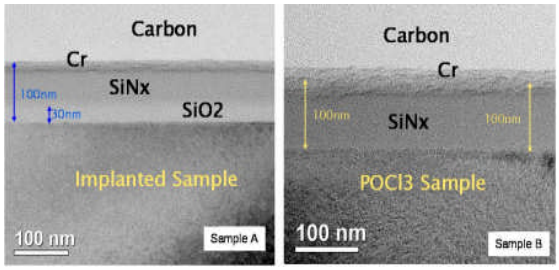

Figure 2. Cross-section TEM comparisons between Implanted and $POCl_3$ emitters illustrating no residual defects in the crystal lattice in the implanted emitter. A smooth Si-SiO_2 interface and the presence of a thin passivating oxide are also evident from the picture.

2.3 Improved Surface Passivation with thermal oxide

Oxide passivation has been used successfully on very high efficiency solar cells including the PERL cell developed by UNSW [15]. Since ion implantation does not require any parasitic dopant containing layers (such as the phosphor-silicate glass in diffusion based processes) it is possible to grow and retain a high quality thermal oxide for implanted emitters without the need for removal/ additional processing in the process flow. Improved surface passivation results in lower recombination currents in the emitter thus enabling a higher Voc entitlement in the finished solar cell. This Voc entitlement is measured after the activation anneal using the quasi-steady state photoconductivity decay (QSSPCD) technique [16]. Implanted emitters (Rsheet =60ohm/sq) result in an excellent implied Voc on 1.7 ohm.cm p-type IPA/KOH Si substrates as shown in Figure 3 below. Implied Voc values >650mV (@1 Sun intensity) are indicative of very low recombination in the emitters due to the excellent surface passivation due to thermal oxide as well as a high bulk lifetime obtained after the anneal.

As further evidence of superior emitter quality, we refer to Figure 4 that shows the QE and reflectance measurements on a 60ohm/sq implanted emitter fabricated using the Solion "Blue" process. The excellent blue response of the cell is indicative of very low recombination in the emitter and excellent surface passivation. The IQE value of >90% for wavelengths in the infrared spectrum (450nm to 950nm) validates that the Solion "Blue" process is capable of delivering high cell performance with a simplified process flow. With a selective emitter process we obtain a further improvement in the blue response and plan to report the results in a future publication.

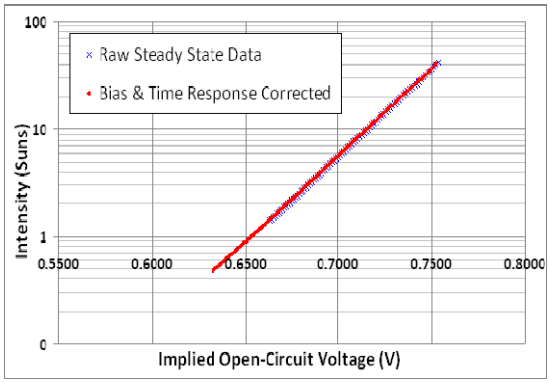

Figure 3. Implied Voc measurements on a 60ohm/sq implanted emitter indicating excellent surface passivation of the emitter and good bulk lifetime obtained after the activation anneal.

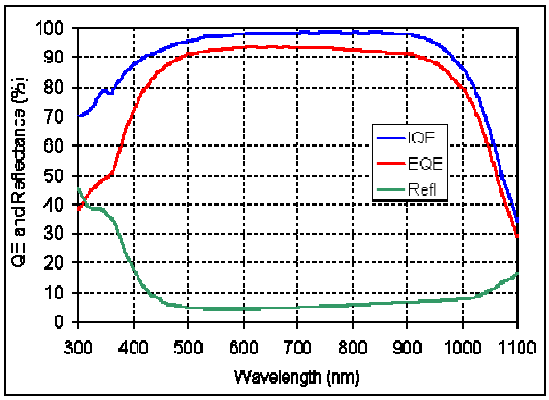

Figure 4 QE and reflectance measurements of a characteristic cell made using the "Blue" Process. The excellent blue and red response indicates excellent surface passivation as well as good bulk lifetimes with implanted emitters.

2.4 Integrated Patterned Doping

A key requirement for integrating selective emitter cells into high volume manufacturing is the capability to form selectively doped regions in a fast and repeatable manner. VSEA's Solion implanter is capable of selectively doping >1000 solar wafers per hour. This is enabled through two implant steps, one to dope the entire wafer surface with a light doping dosage and selectively doping the contact regions through the use of an in-situ proximity mask integrated into the implanter. The wafers are implanted in two steps in the implant process. In the first step, the wafers are scanned through a parallel ribbon beam to create the field doped regions. A proximity mask is then inserted between the wafers and the ion beam. This mask defines the regions on the wafers that will get the additional doped in the selective emitter structure. The wafers are then implanted a second time to complete the selective doping in the implanter.

This approach enables the high throughput for the implant process and delivers a selective emitter solution at the lowest cost.

An additional issue to be addressed for high volume manufacturing of selective emitter cells is the alignment requirements between the heavily doped regions with the front metal grid on the screen printers adding to the cost of manufacturing for selective emitter cells. The Solion "Blue" process also enables simpler alignment options between the implanted regions and existing screen printer using either "reference edge alignment" or direct optical alignment using the contrast between the heavily doped and lightly doped regions that originates from doping dependent oxidation rates of Silicon. The oxide thickness is a strong function of the dopant dose and hence the oxide layer grown on the heavily doped contact regions is thicker than the oxide that grows on the lightly doped field regions during the same anneal. This difference in oxide thickness in different regions enhances the contrast between the heavily doped and lightly doped regions even after the SiN layer is deposited making the regions distinguishable to the naked eye and enabling automated optical alignment on the screen printers using standard camera based optical alignment systems. This greatly simplifies the alignment process in the manufacturing flow and is also highly repeatable. In order to alleviate the need for optical alignment on the screen printer, VSEA have also developed and tested an alternative approach of using a reference edge on the wafers for alignment of the selectively doped regions on the implanter and using the same edge as a reference on the screen printer. The experimental details and results from these alignment verification tests have been reported previously [11] and indicate that such a method is well suited for use in mass production.

3 EXPERIMENTAL RESULTS

Fully implanted selective emitter solar cells were fabricated on p-type CZ wafers (B-doped, bulk resistivity between 1.5 to 2.5Ω.cm, thickness ~200µm, 156mm x 156mm pseudo-square) using standard solar cell processing with screen printed Front Ag Grid and Al-BSF (with Ag Back Busbars). The as-cut wafers go through saw-damage etch followed by a KOH/IPA texture etch to form random upright pyramids on both sides The wafers are then implanted in two chained implant steps on the same sides to form the selectively doped emitter regions. The doping level in the emitter regions is optimized via precision doping enabled by ion implantation to eliminate the "dead" layer (commonly seen in $POCl_3$ emitters) resulting in a high quality emitter layer. The implanted wafers then go through a dry oxidation anneal at typical temperatures of 800-900C to result in 10-20nm of thermal oxide in the lightly doped emitter regions. The resulting sheet resistance values for the lightly doped emitter region are typically 80 to 120 Ohm/Sq., while the contact regions are 50 to 60 Ohm/Sq. A thinner PECVD SiNx layer is then deposited on top of the oxide to minimize the reflectance from the frontside of the cells. The optimum SiNx thickness has been determined through a few SiNx thickness splits. The results of such an optimization are contingent on the specific optical properties (n, k) of the SiNx layer being deposited but one such optimization is illustrated in Table1, where the optimum SiNx thickness (for minimum reflectance) is listed for several different SiO2 thicknesses. Generally, the total thickness of the optimum ARC stack stayed unchanged in the experiment i.e., t(SiO2) + t(AR SiN) ~85nm.

Table I. Optimized SiNx thickness for different oxide thicknesses on the emitters

t(SiO2) [nm]	t(AR SiN) [nm]
34	47
10	75
7	80
3	80

The two regions of the selective emitter are also optically visible enabling easy alignment between the screen printed metal fingers and the heavily doped contact regions. The front and back metal contacts are printed on an ASYS screen printer. The front Ag paste (9235HM) and the back busbar paste (SOL230) are available commercially from Heraeus while the back Al paste (RX8252X) used in our experiment is available from Ruxing. The triple BBR front grid pattern was optimized for the selective emitter design to minimize the total power losses from the cell (resistive + shading). Front and back contacts were printed, dried and co-fired in a belt furnace with temperature profile in the firing furnace optimized to make low resistance contacts to the emitter. Figure 4 shows a camera image of a finished selective emitter cell, showing the contrast between the lightly doped field regions and more heavily doped contact regions. The key to this origin of this contrast is the dopant dependent oxidation rate, leading to slightly thicker oxide over the more heavily doped regions. While there is no impact to metal contacting, the visible selective implants aid optical alignment to the metal at the screen printer. The image shown here has a wider linewidth to highlight the contrast between the selectively doped regions and illustrate th edge alignment method. Further optimization of mask geometry and alignment approaches will be reported in the future.

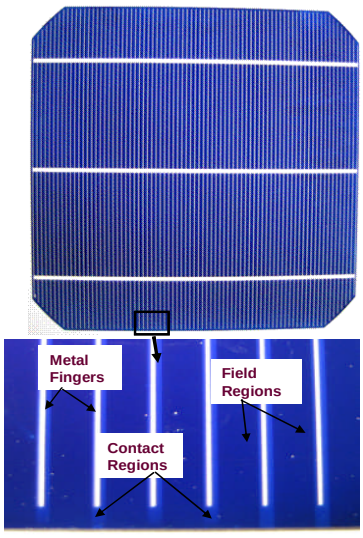

Figure 4. Optical camera image of a finished selective emitter cell showing the contrast in the differentially doped regions of the cell

Table II : Summary of Cell IV characteristics obtained of 239cm^2 area p-Cz material

	Cell Efficiency (%)	Jsc (mA/cm^2)	Voc (V)	FF (%)
Best Cell	18.8	37.3	0.643	78.4
Average (50 cells)	18.5	37.1	0.640	78.0
Standard Deviation	0.14	0.15	0.002	0.4

The light IV measurements of 50 cells processed in the same manner as described above are summarized in Table II. The cells averaged an efficiency of 18.5% with the best cell measuring 18.8%. The tight distribution in all the different cell parameters demonstrates the superior process control enabled via the Solion "Blue" Process.

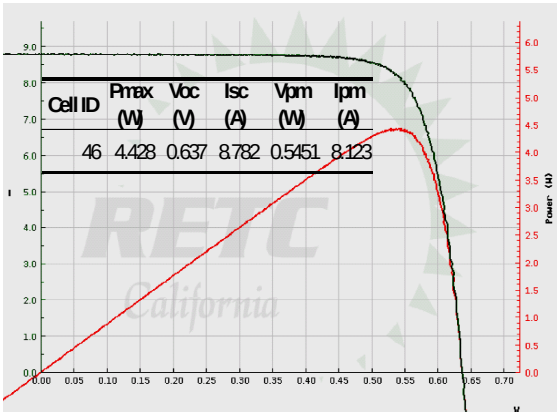

Figure 5 IV characteristic of a characteristic cell made using ion implantation verified by RETC in California.

A typical cell IV curve (certified at RETC, California) is also shown in Figure5. The peak power output of this cell is 4.428W which equates to 18.5% CE. The excellent Voc of 637mV measured on this cell illustrates the superior emitter quality as well as excellent surface passivation.

4 SUMMARY AND OUTLOOK

In this paper, we have introduced a novel manufacturing process based on high throughput (>1000 wph), in-situ patterned ion implantation for the doping step. The approach is shown to boost the cell performance on standard p-Cz cells with a simplified process flow. The key benefits for improving cell efficiency are a) Process Simplification through elimination of PSG strip and Junction Isolation steps b) improved quality of junction doping (e.g. elimination of dead layer), c) improved surface passivation through the integration of thermal oxidation in the process flow, and d) in-situ patterned doping for advanced cell architectures such as selective emitter. The Solion "Blue" process is shown to deliver >18.5% CE average and may be optimized further to boost the average cell performance to 19%. Patterned ion implantation addresses the need for single-sided patterned doping for both p and n-type dopants and thus enables cost effective manufacturing of many advanced cell structures such as IBC and other high efficiency cells that will lead c-Si based PV to grid parity.

5 ACKNOWLEDGEMENTS

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